



Compal Confidential

Schematics Document

Intel

U3HR

LA-6691P

2011-03-07

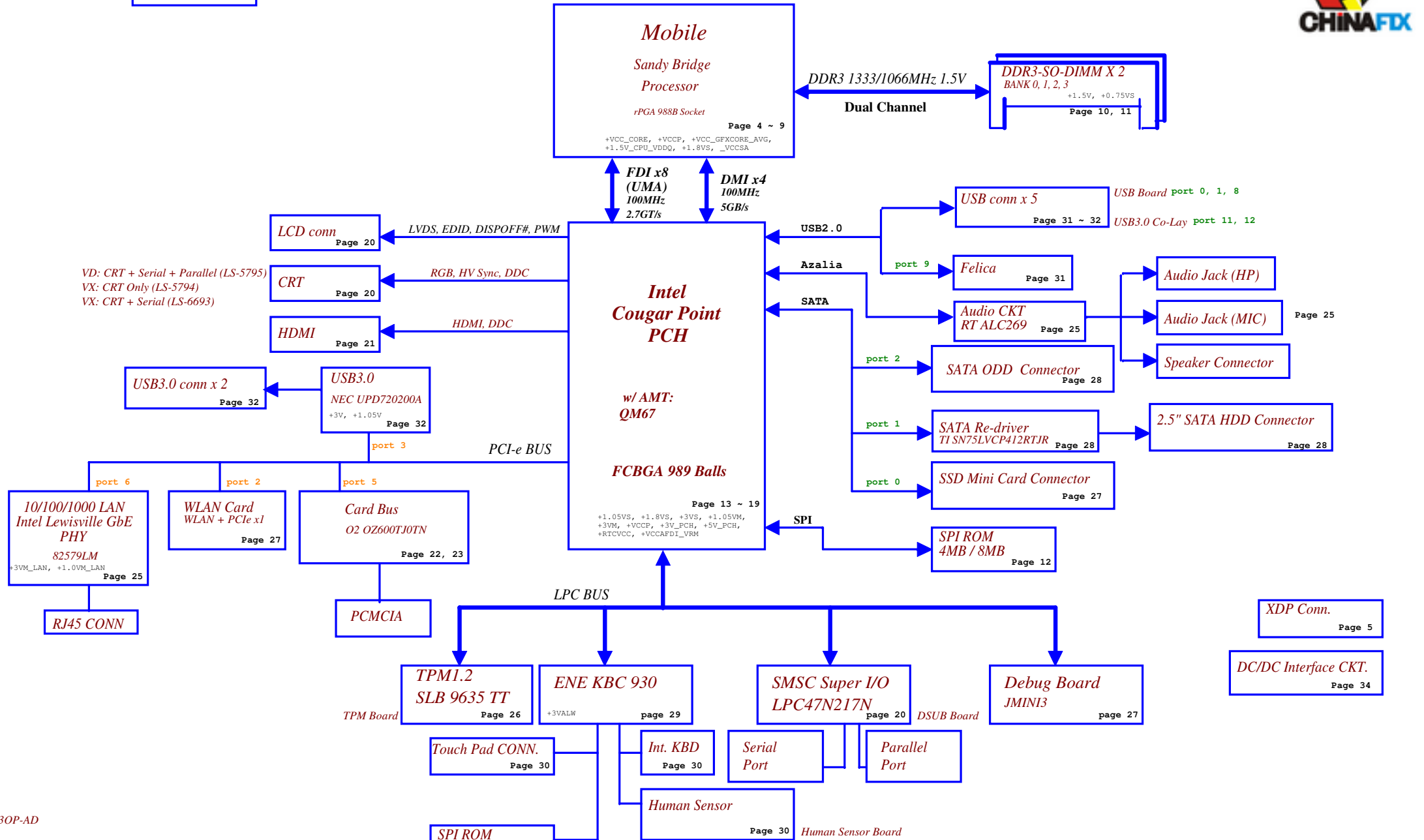
REV: 0.6

Security Classification		Compal Secret Data		Title	
Issued Date	2010/09/30	Deciphered Date	2011/12/31	Cover Sheet	
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Fan Control
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U3HR



Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	+B +3VL	+5VALW +3VALW	+3V_PCH	+1.05VM_LAN +3VM (SLP_LAN#)	+1.05VM (SLP_A#)	+1.5V +3V	+5VS +3VS +1.5VS +VCC_GFXCORE +VCCP +CPU_CORE +1.8VS +1.05VS +0.75VS +VCCSA
S0	O	O	O	O	O	O	O	O
S3 / DC & no WOL	O	O	O	O	X	X	O	X
S3 / DC & WOL	O	O	O	O	O	X	O	X
S3 / AC & PP1 & no WOL	O	O	O	O	X	X	O	X
S3 / AC & PP1 & WOL	O	O	O	O	O	X	O	X
S3 / AC & PP2 (M3)	O	O	O	O	O	O	O	X
S3 / AC & PP2 (Moff)	O	O	O	O	O	X	O	X
S4 S5 / DC & no WOL	O	O	X	X	X	X	X	X
S4 S5 / DC & WOL	O	O	O	O	O	X	X	X
S4 S5 / AC & PP1 & no WOL	O	O	O	O	X	X	X	X
S4 S5 / AC & PP1 & WOL	O	O	O	O	O	X	X	X
S4 S5 / AC & PP2 (M3)	O	O	O	O	O	O	X	X
S4 S5 / AC & PP2 (Moff)	O	O	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	EXPRESS CARD	LAN CHIP	EC-KB930
<div>SMB_EC_CK1</div> <div>SMB_EC_DA1</div>	EC	V	X	X	X	X	X	X
<div>SMBCLK</div> <div>SMBDATA</div>	PCH	X	V	V	V	V	X	X
<div>SML0CLK</div> <div>SML0DATA</div>	PCH	X	X	X	X	X	V	X
<div>SML1CLK</div> <div>SML1DATA</div>	PCH	X	X	X	X	X	X	V

Symbol Note :



: means Digital Ground



: means Analog Ground



Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.5

VD: VD@+USB3@+KB@

VX: VX@+USB2@+KB@

VX/10key: VX@+USB2@+10KB@

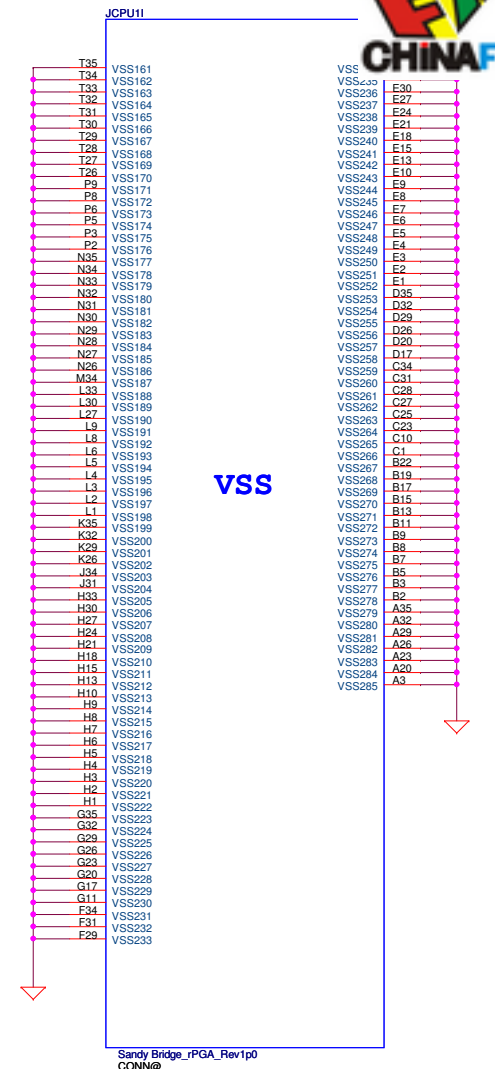
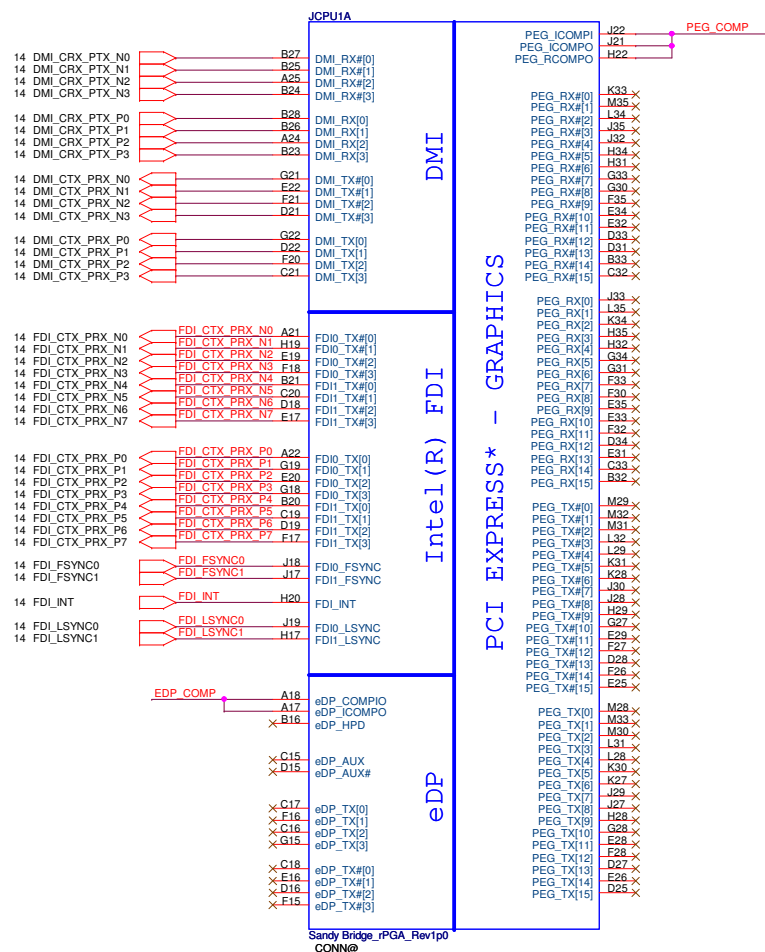
@ : means just reserve , no build

CONN@ : means ME part.

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	3.3K +/- 5%	0.0908 V	0.1054 V	0.121 V
2	6.8K +/- 5%	0.1817 V	0.2101 V	0.2422 V
3	10K +/- 5%	0.2601 V	0.3 V	0.3448 V
4	15K +/- 5%	0.3746 V	0.4304 V	0.4927 V
5	20K +/- 5%	0.4974 V	0.55 V	0.6076 V
6				
7				

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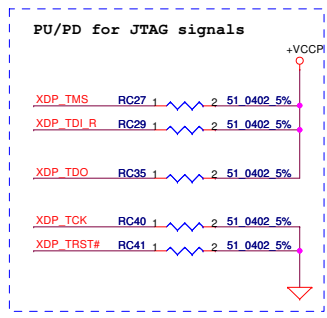
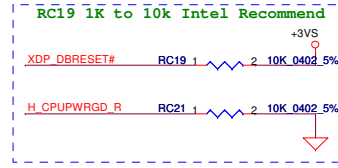
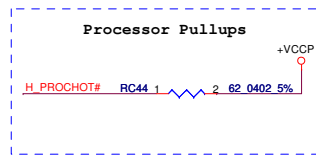
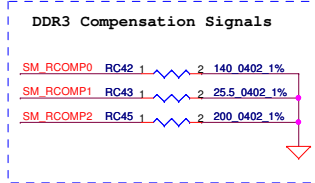
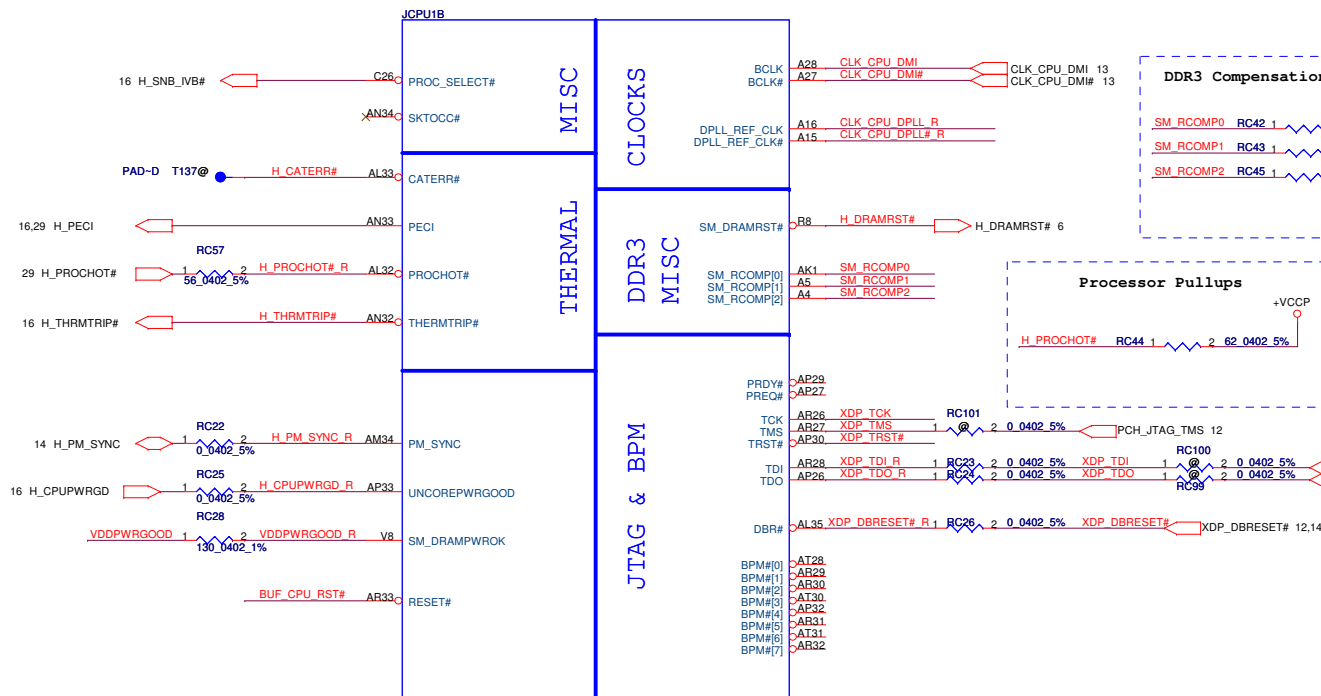
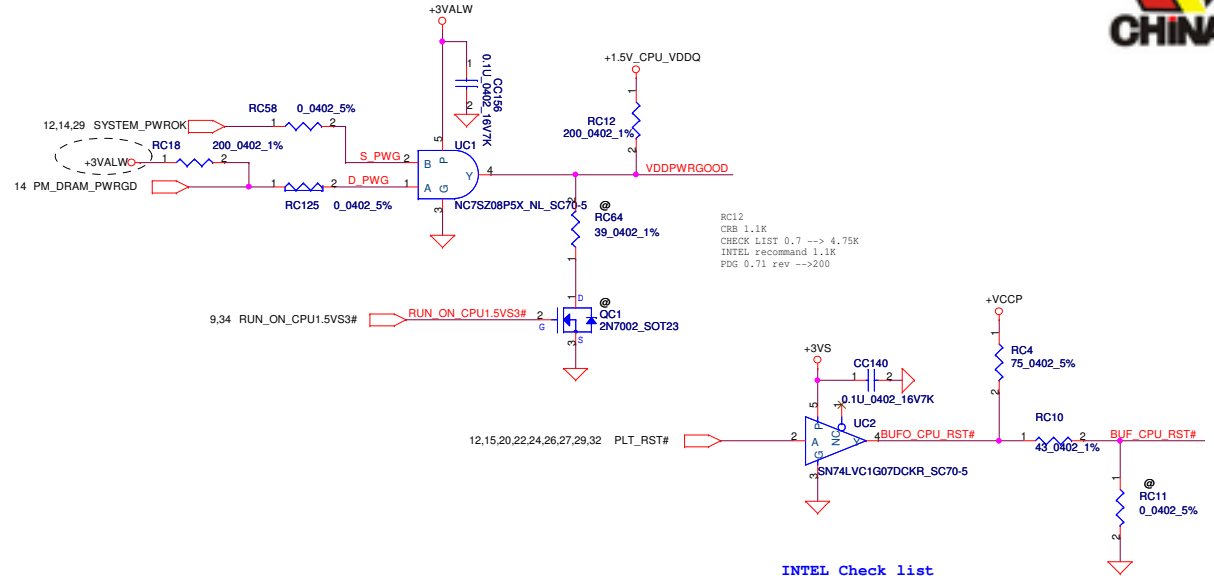


PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

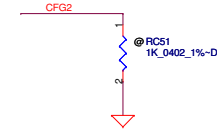
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Issued Date	2010/09/30	Deciphered Date	2011/12/31	Title	PROCESSOR(1/6) DMI,FDI,PEG
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Remove XDP CONN for MRT BRD



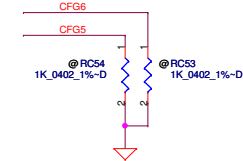
1

CFG Straps for Processor



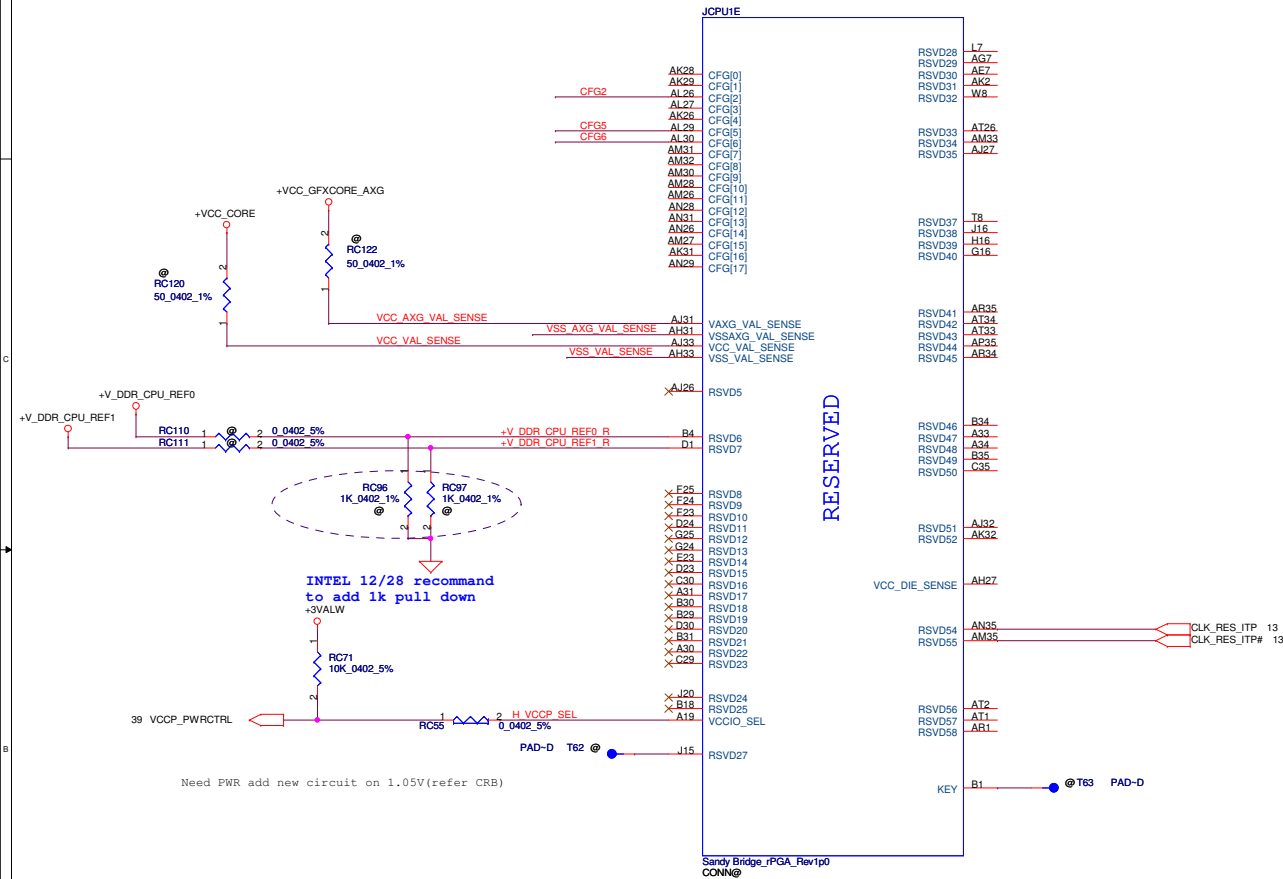
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	--

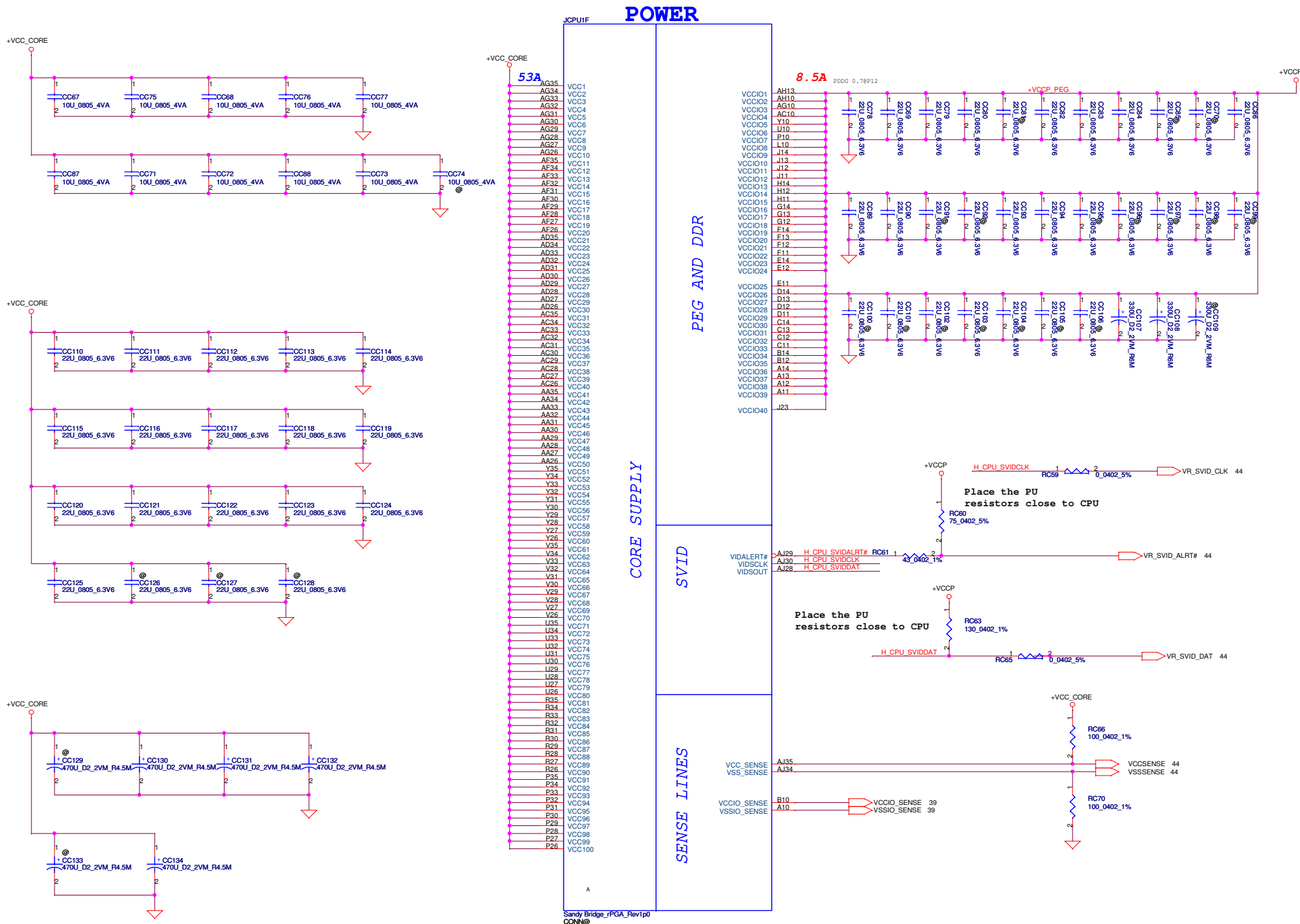


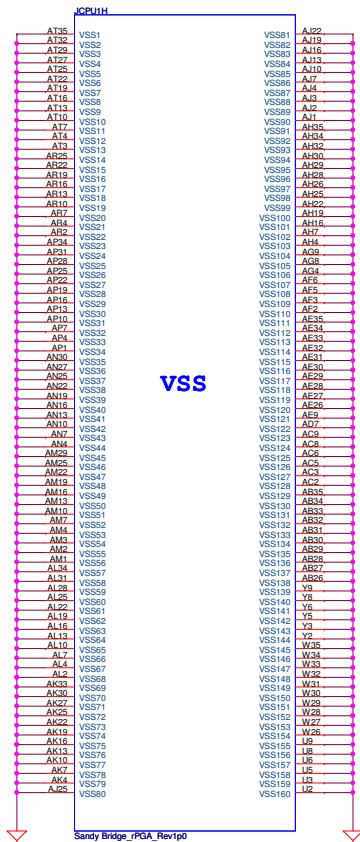
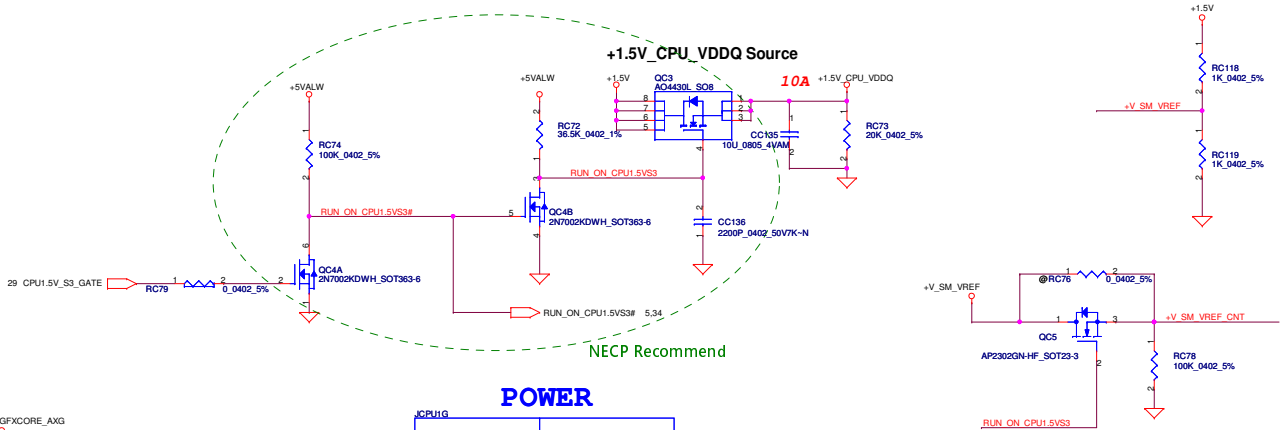
PCIe Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
----------	--



INTEL 12/28 recommend
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1





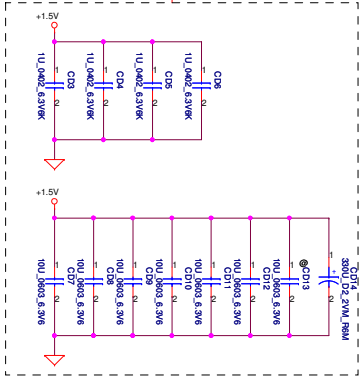
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Issued Date	2010/09/30	Deciphered Date	2011/12/31	Size	
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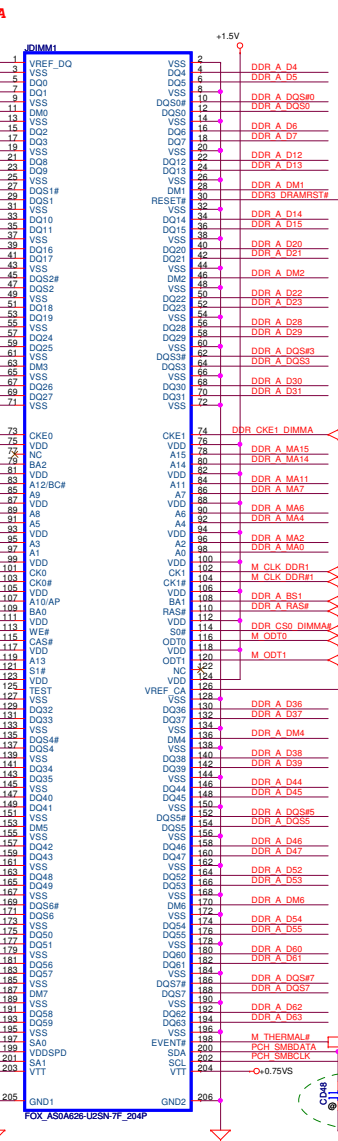
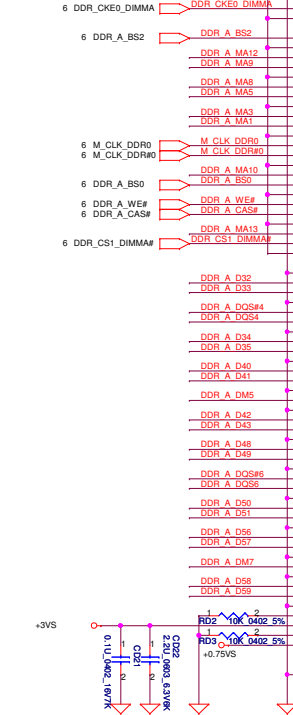
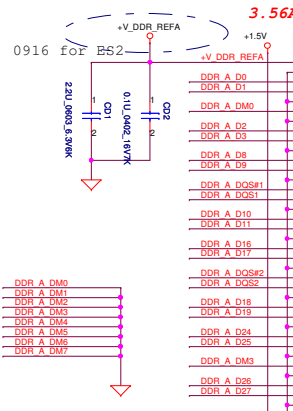
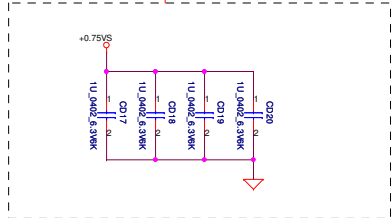
6 DDR_A_DQS[0..7]
6 DDR_A_DQS[8..7]
6 DDR_A_D[0..63]
6 DDR_A_MA[0..15]

All VREF traces should
have 10 mil trace width

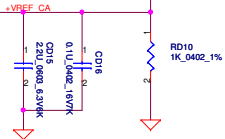
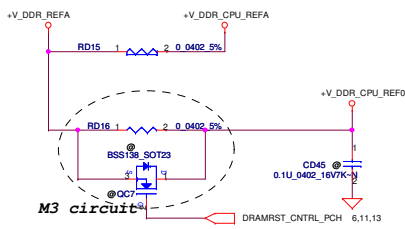
Layout Note:
Place near JDIMM1



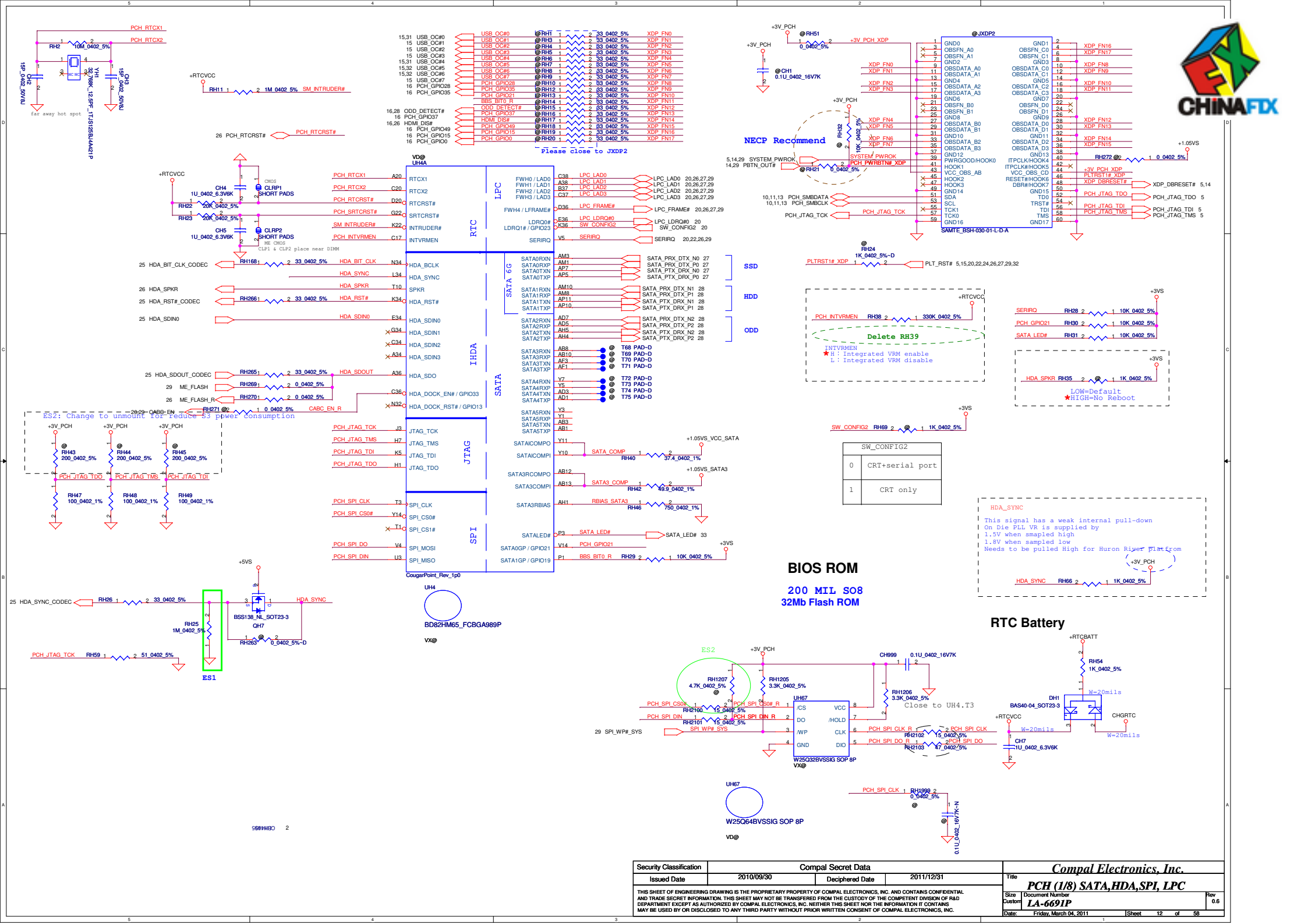
Layout Note:
Place near JDIMM1.203,204

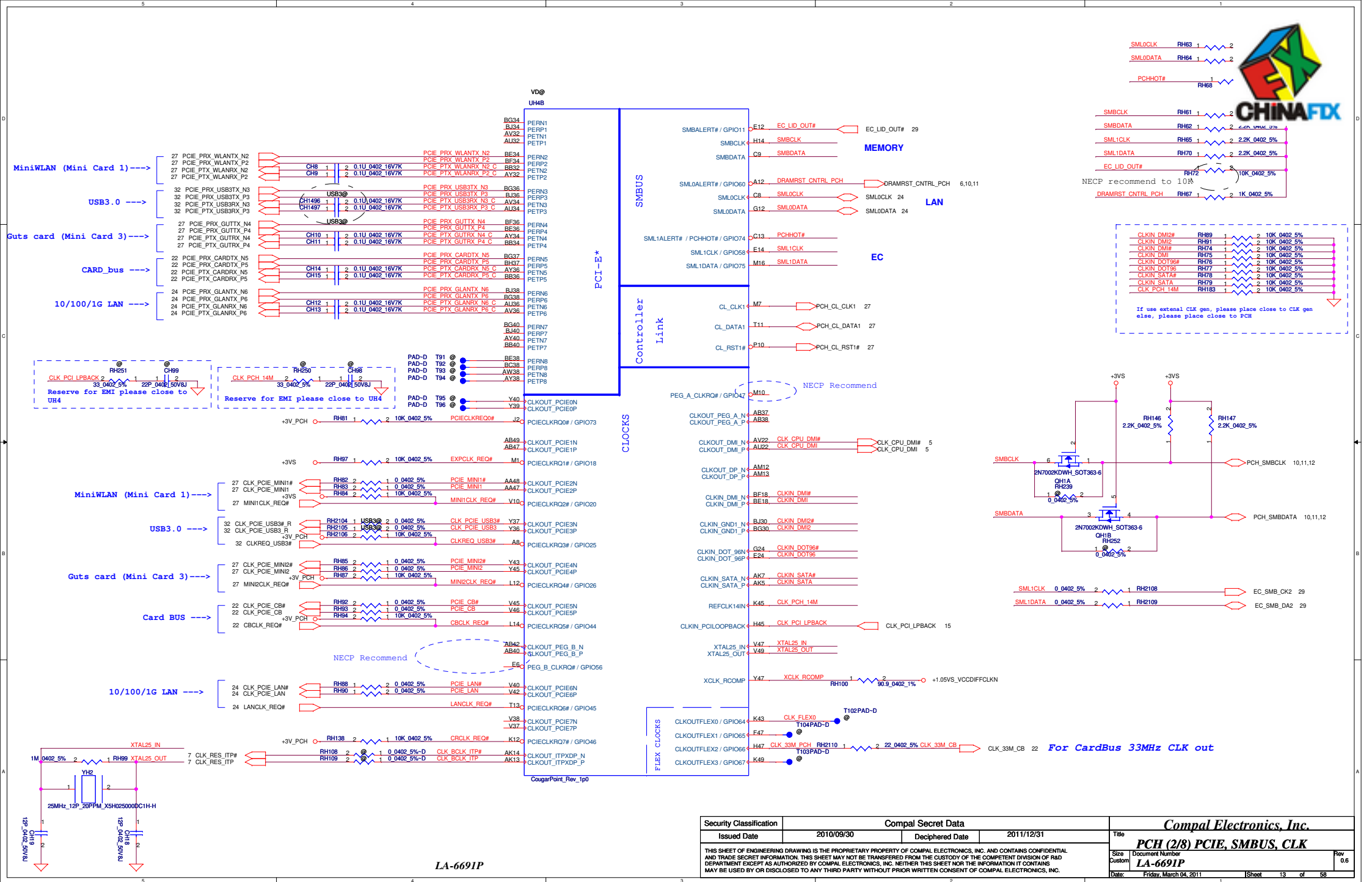


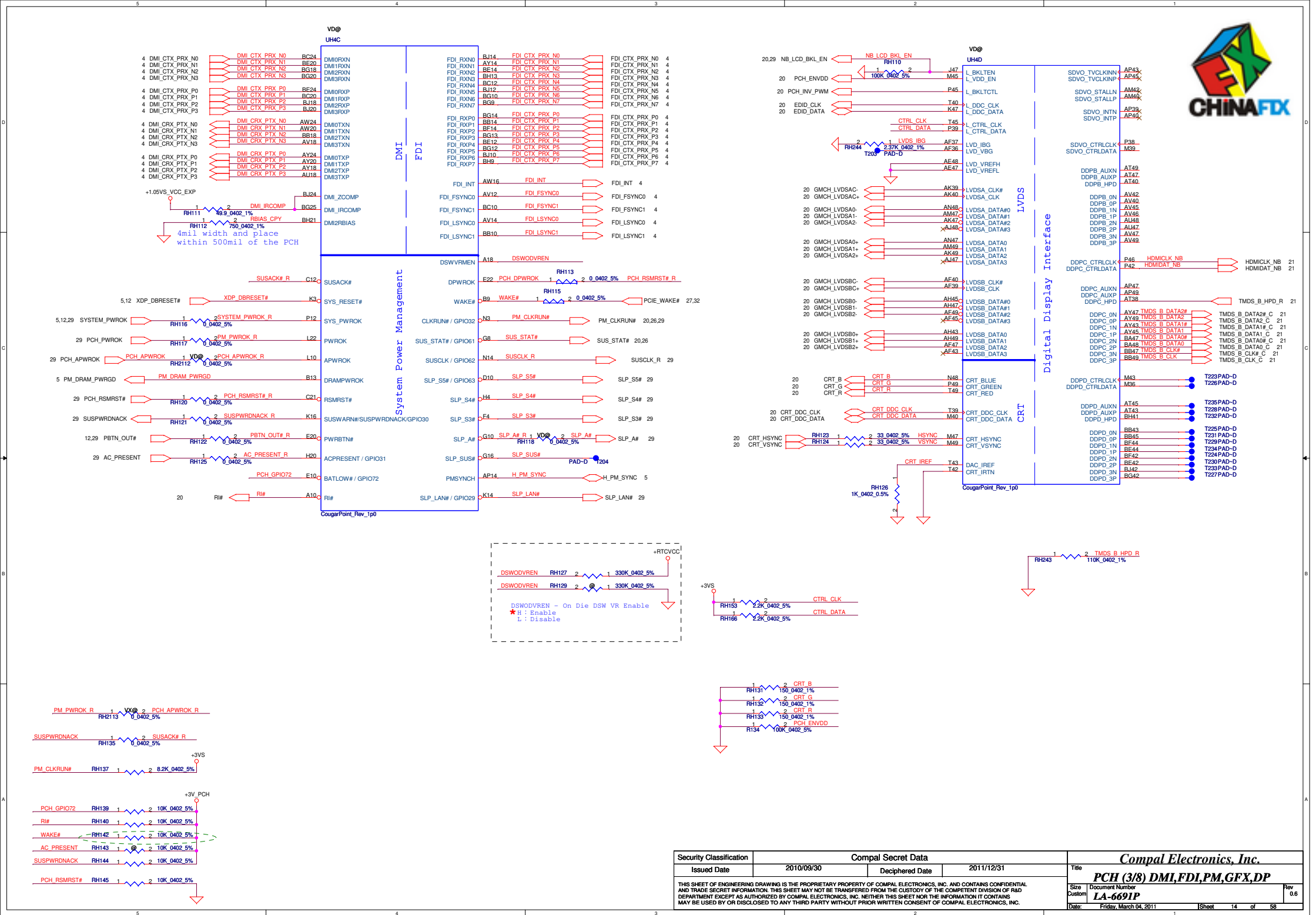
JDIMM H=5.2

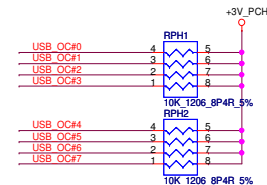
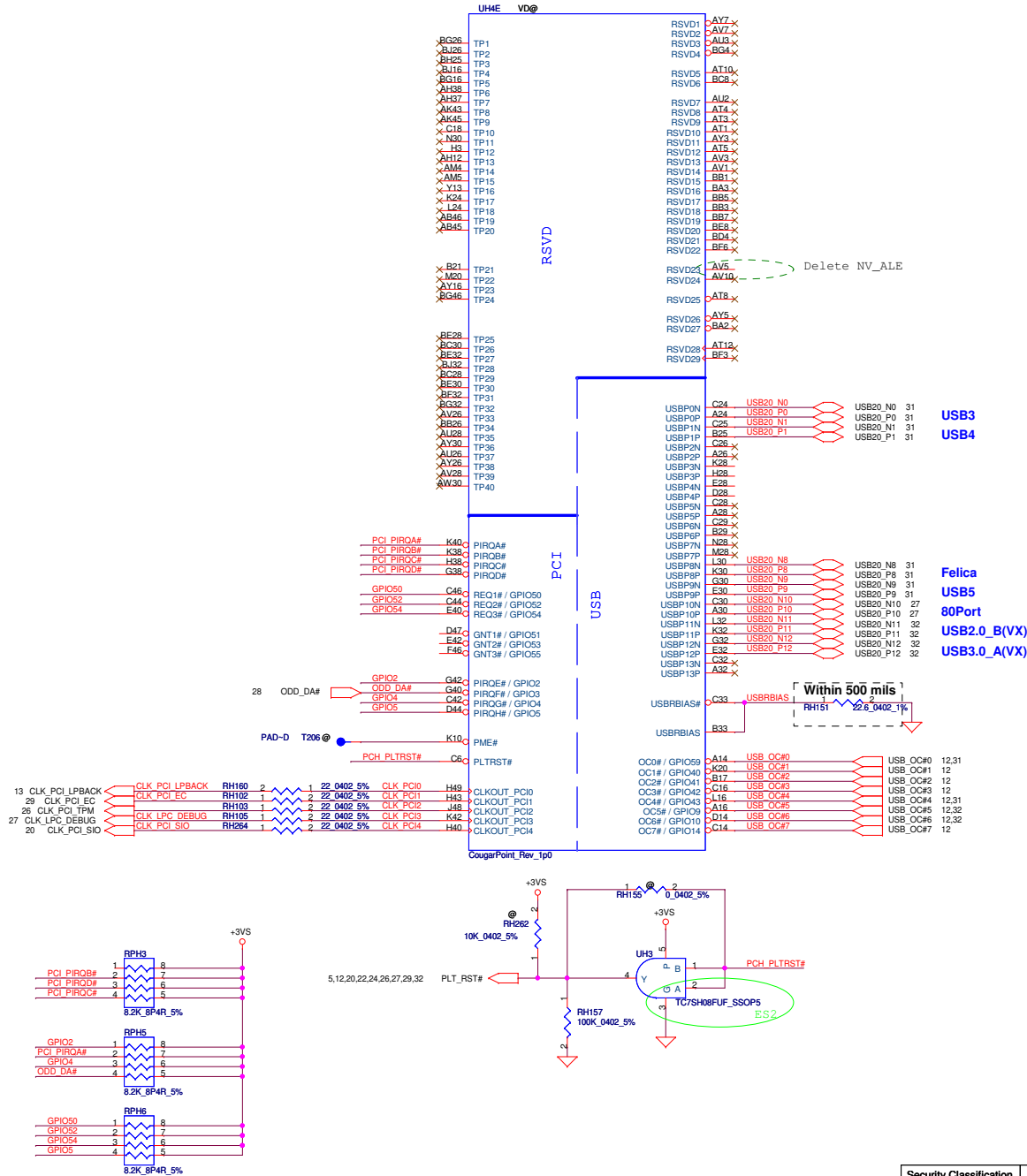


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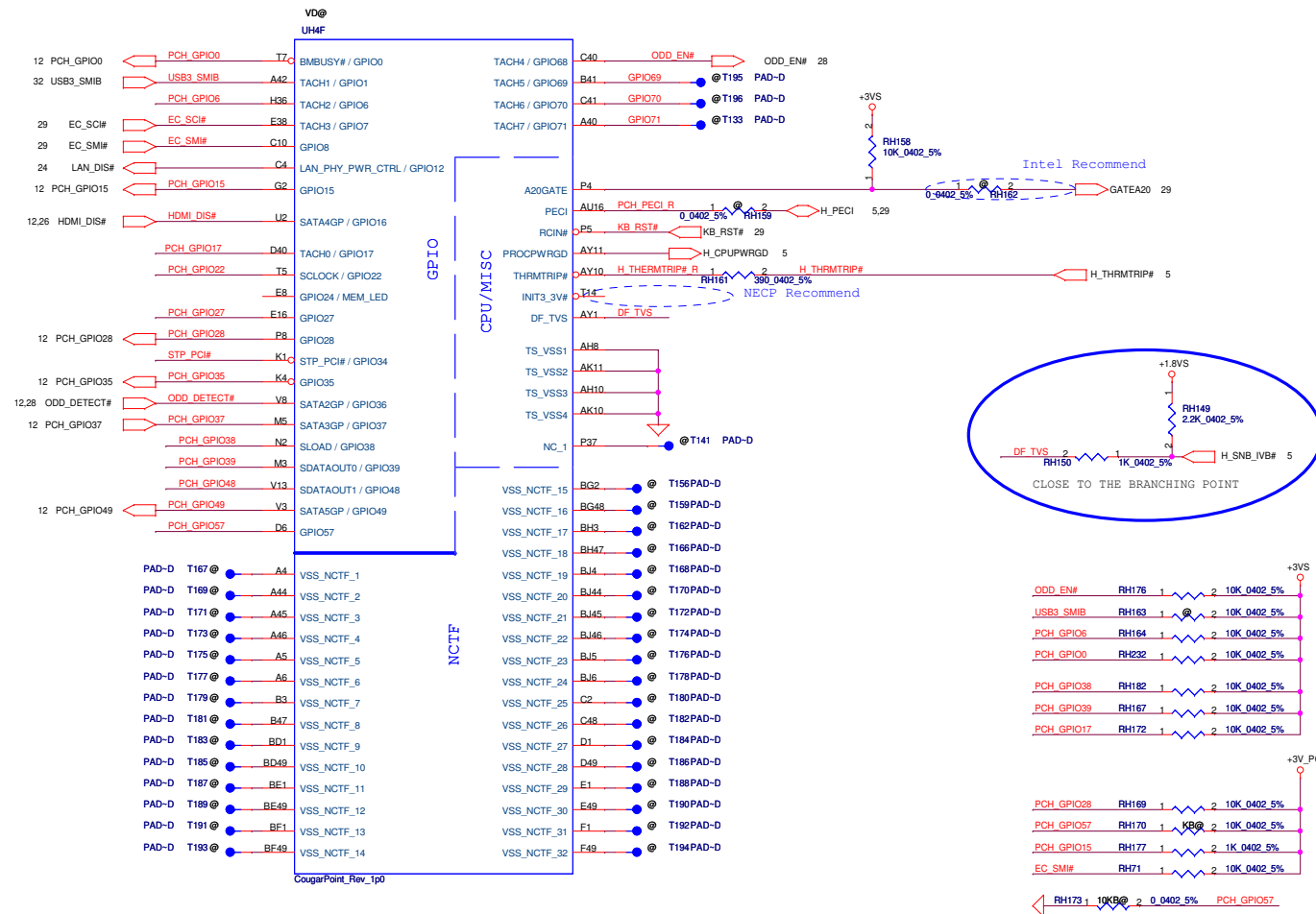
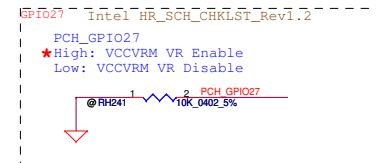
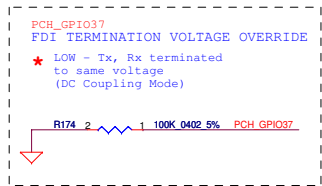
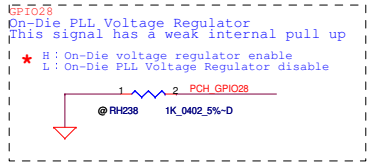




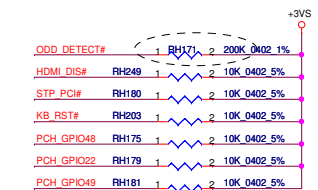


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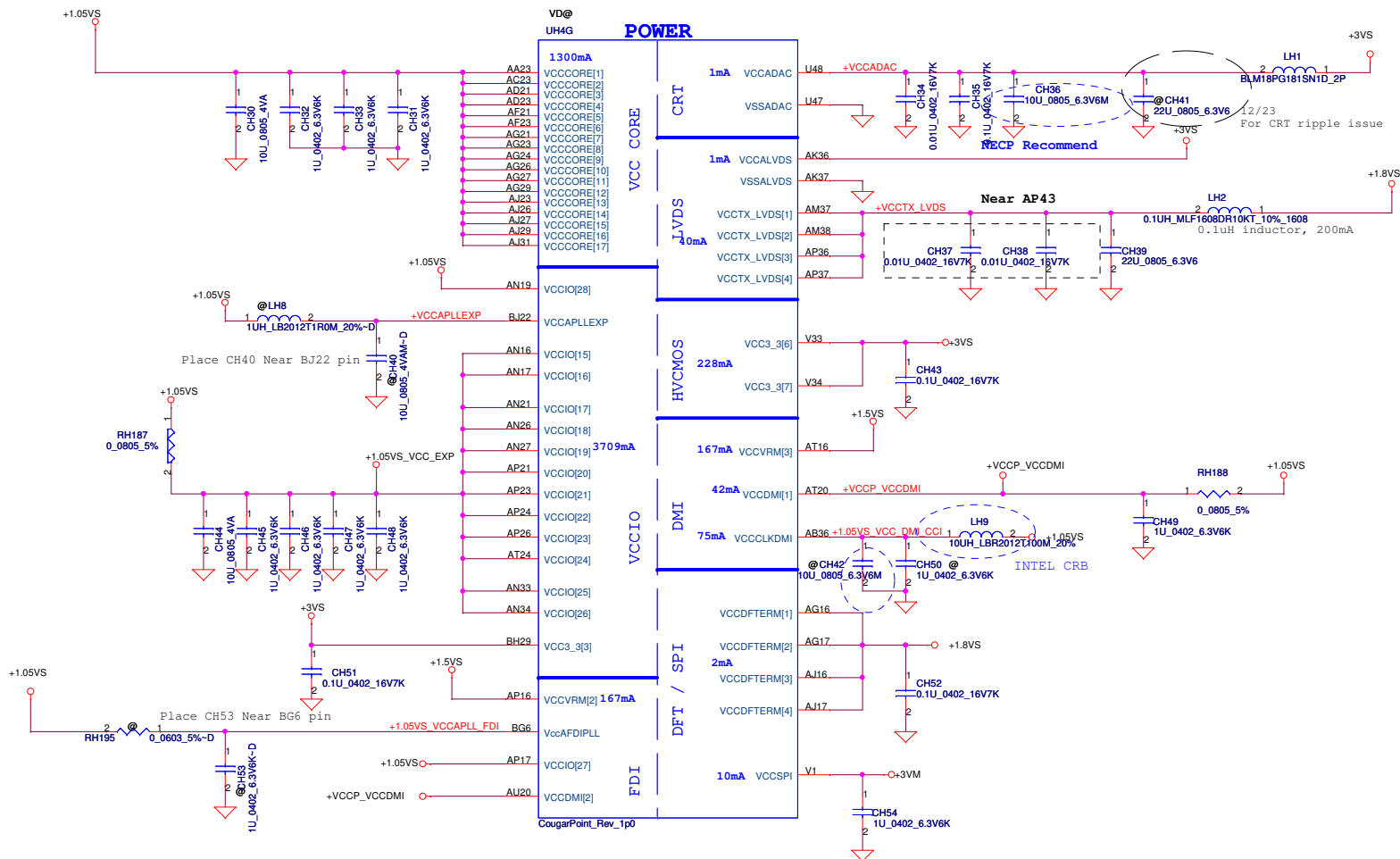
	W/10-key	WO/10-key
PCH_GPIO57	0	1



```
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0
```

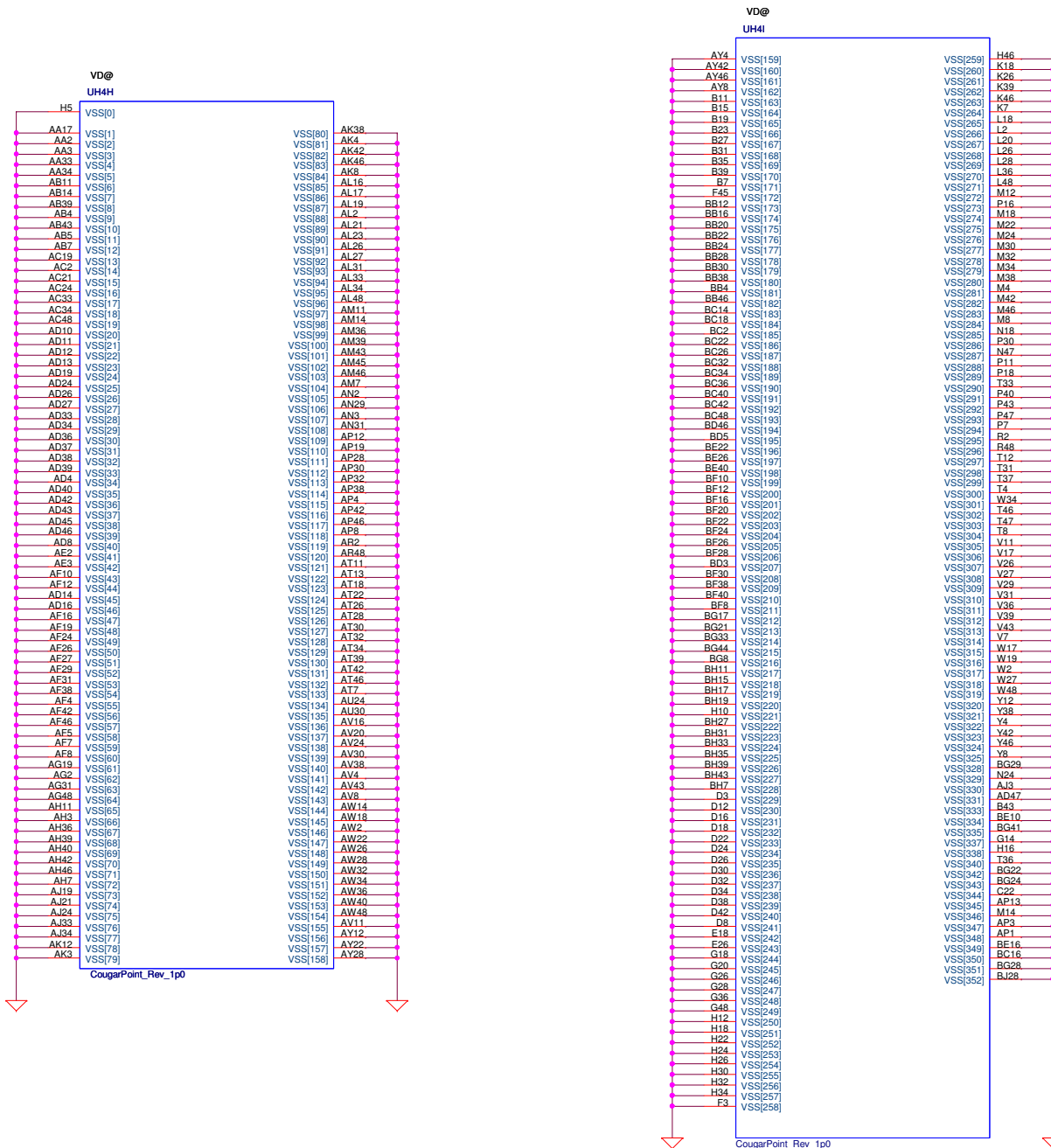
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PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detal waiting for newest spec

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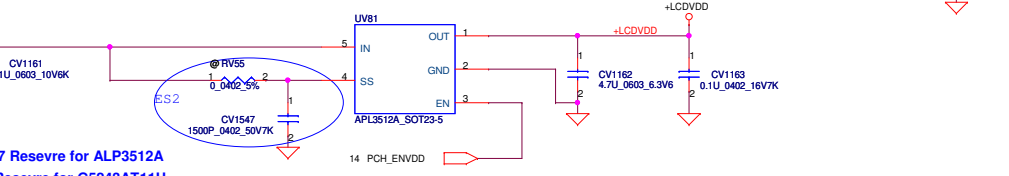
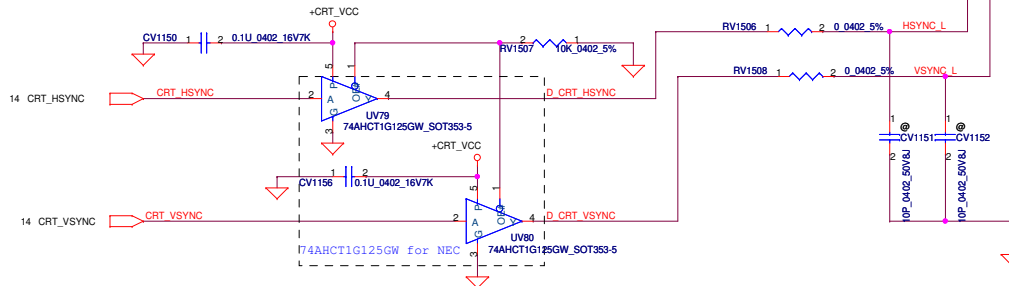
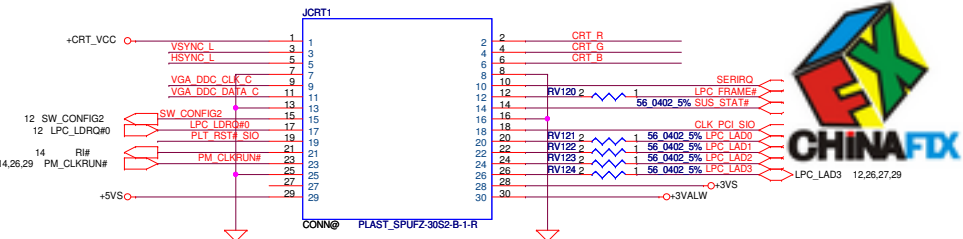
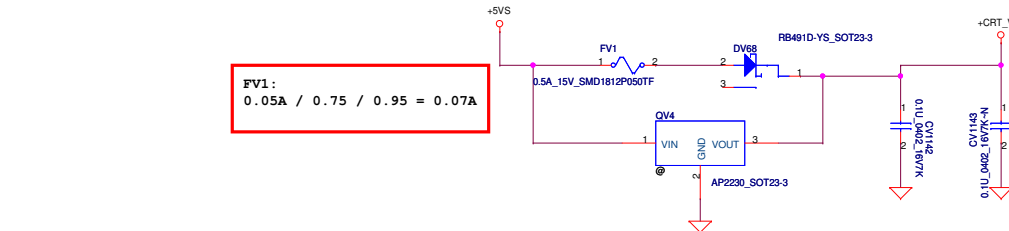


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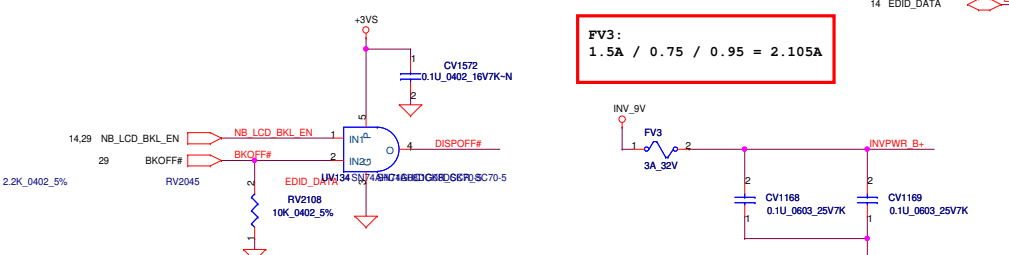
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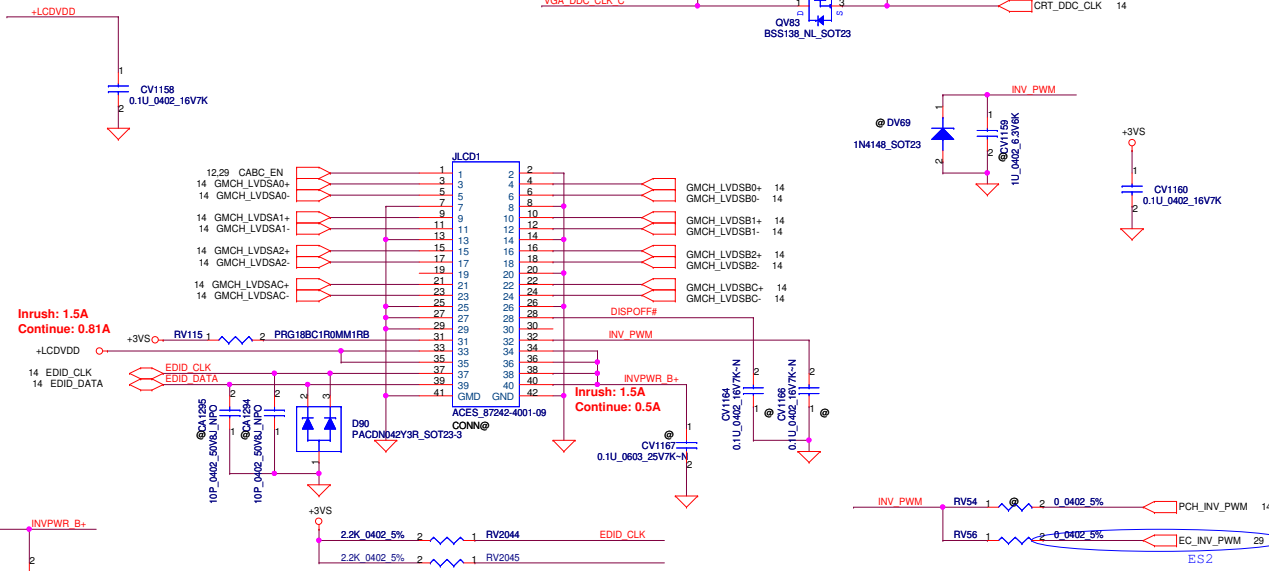
FV1:
0.05A / 0.75 / 0.95 = 0.07A



CV1547 Resevre for ALP3512A
RV55 Resevr for G5243AT11U

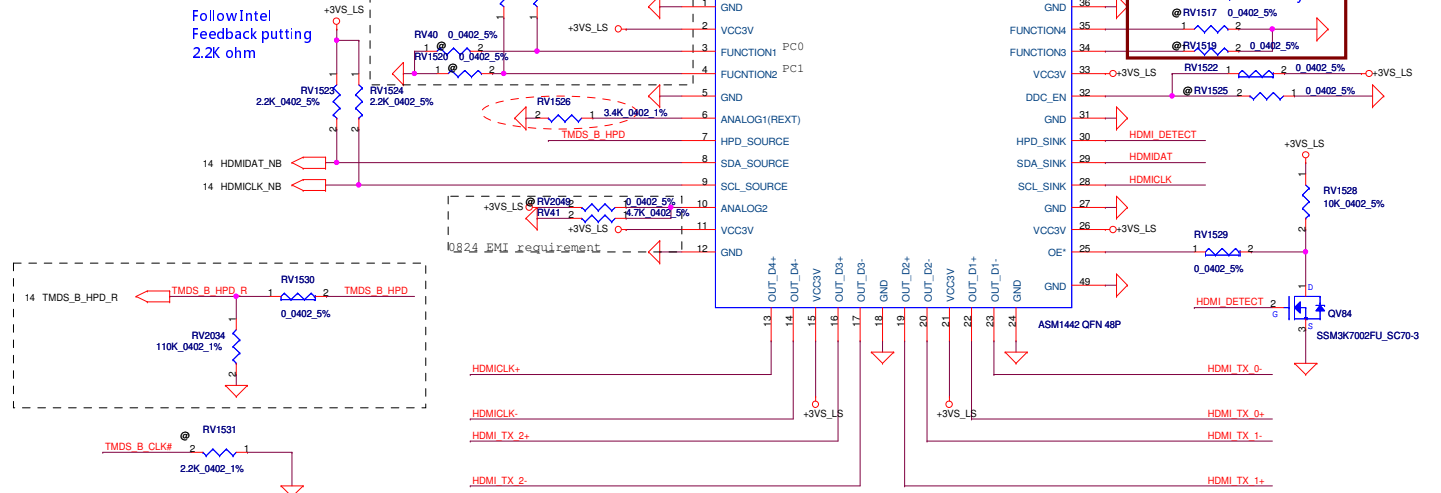
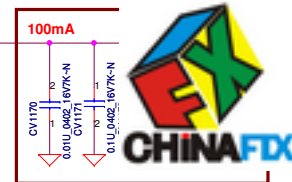


FV3:
1.5A / 0.75 / 0.95 = 2.105A

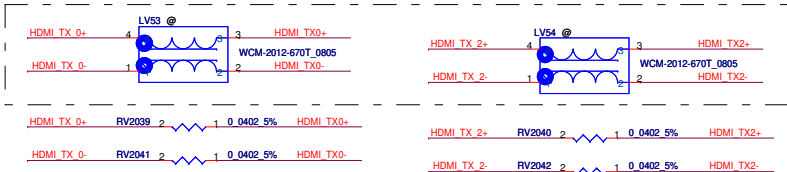
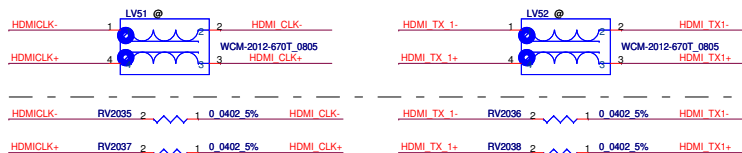


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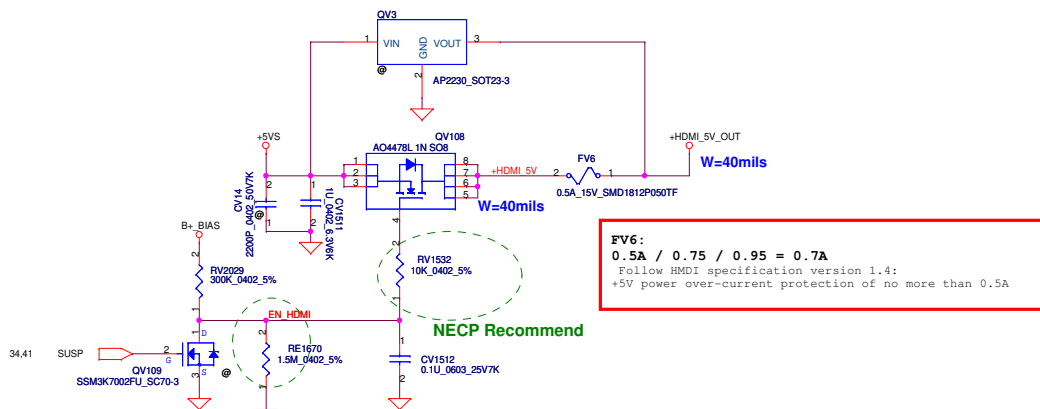
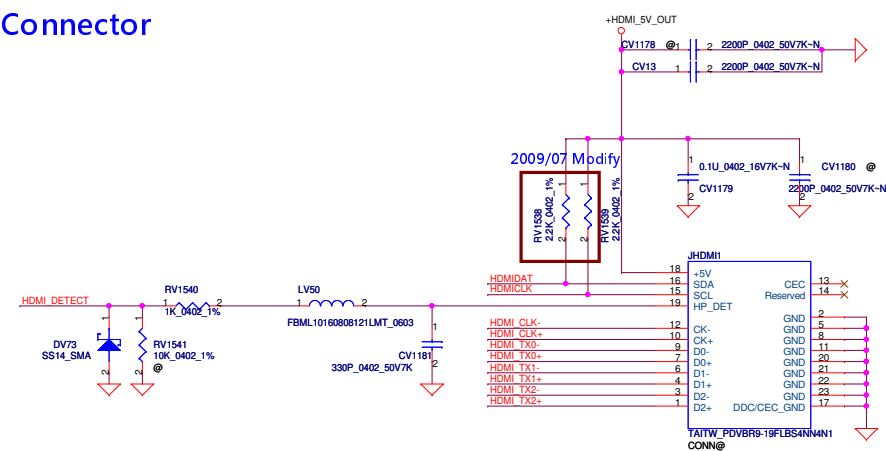
EQUALIZATION SETTING:
[PC1,PC0]=00,8dB
[PC1,PC0]=01,4dB (Recommended)
[PC1,PC0]=10,12dB
[PC1,PC0]=11,0dB



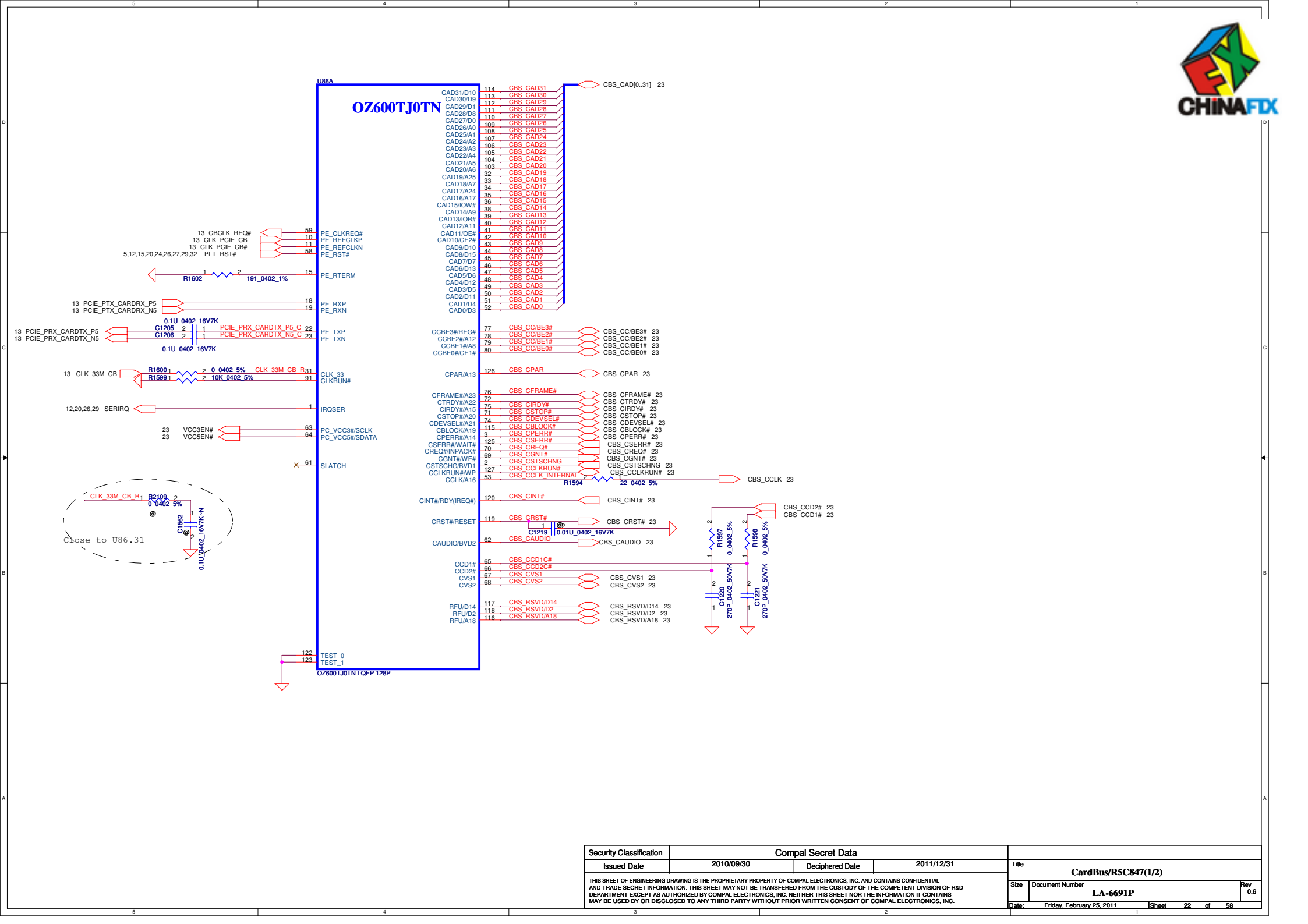
Co-layer for EMI

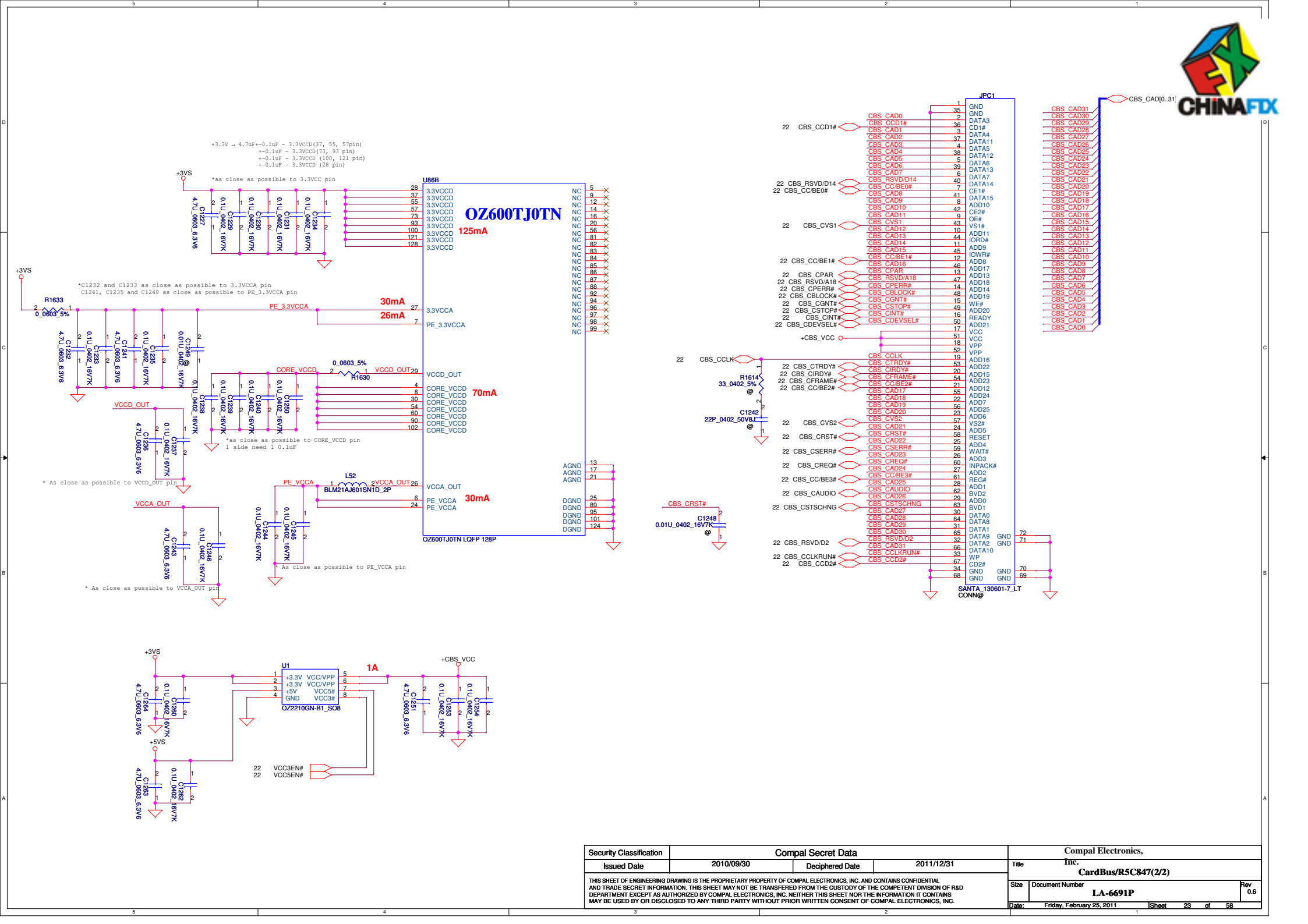


HDMI Connector



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Title		Compal Electronics, Inc.	
Size		HDMI LS & Conn.	
Document Number	LA-6691P	Rev	0.6
Date	Friday, February 25, 2011	Sheet	21 of 58

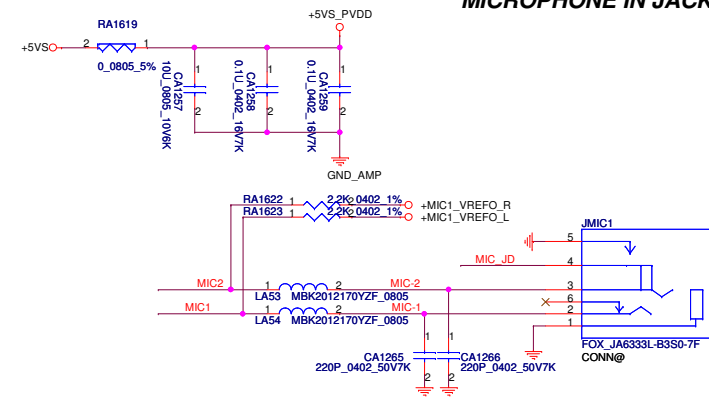




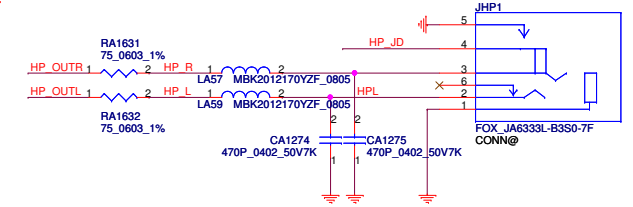
Security Classification	Compal Secret Data			Compal Electronics, Inc. Intel 82579 Niveveh		
Issued Date	2010/09/30	Deciphered Date	2011/12/31	Title		
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					LA-661P	0.6
				Date:	Friday, March 04, 2011	Sheet 24 of 58



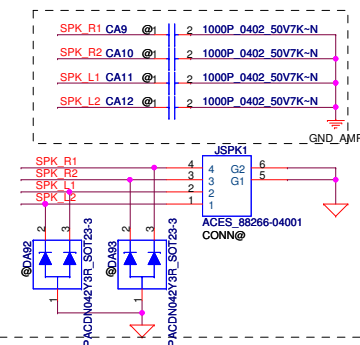
MICROPHONE IN JACK



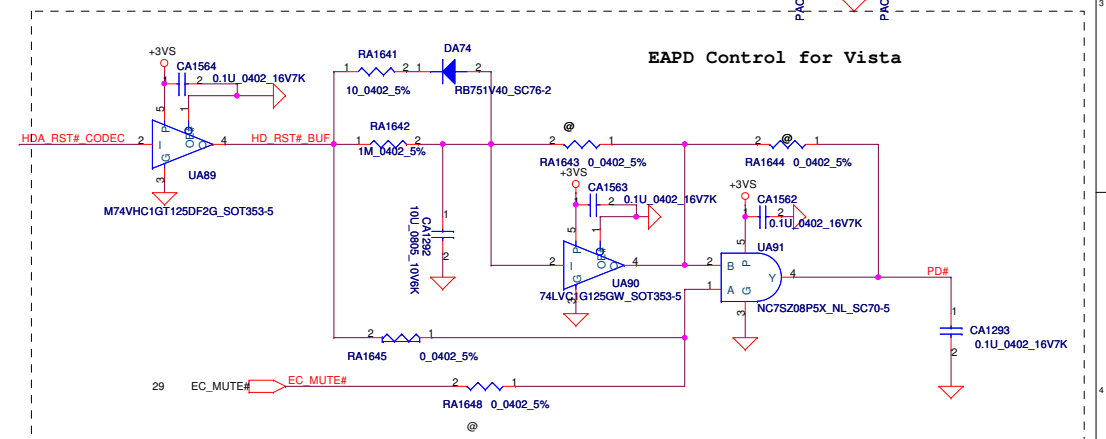
HEADPHONE OUT JACK



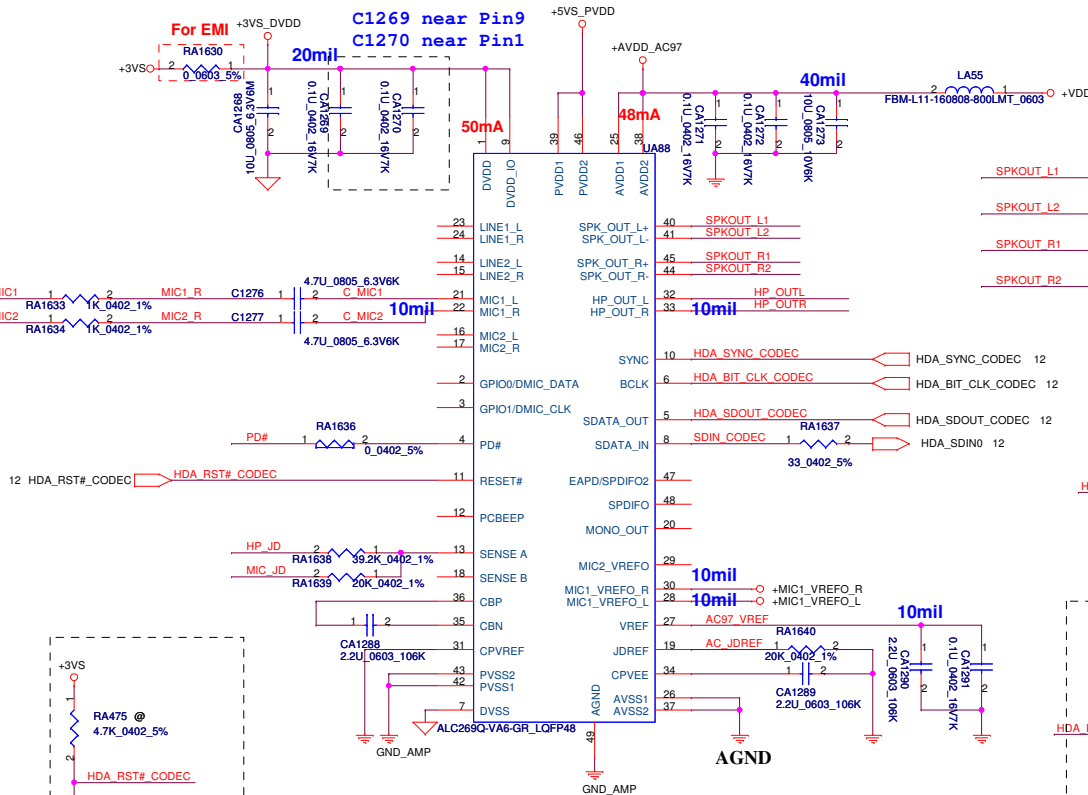
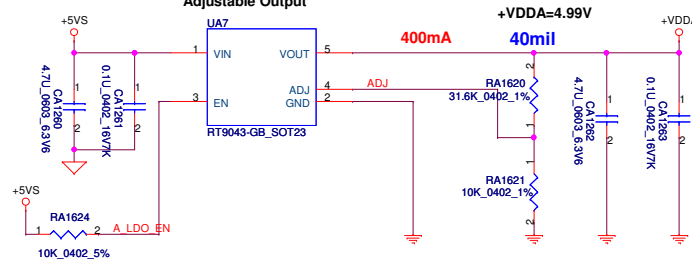
Speaker Connector



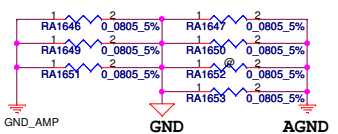
EAPD Control for Vista



Adjustable Output

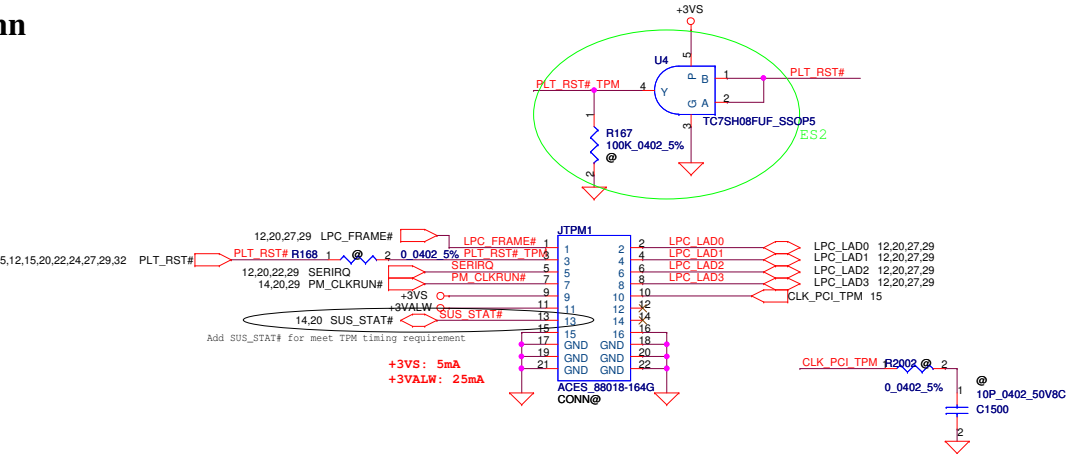


Reserved for TEST



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2011/12/31				2011/12/31				2011/12/31			
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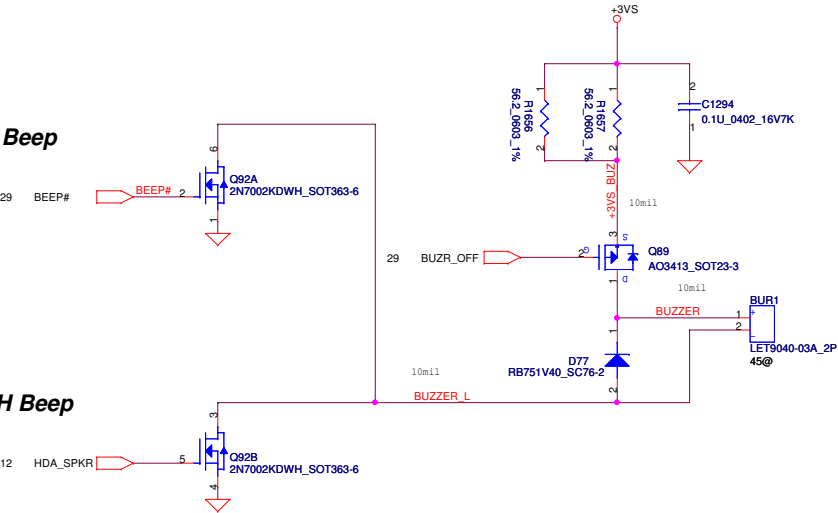
TPM 1.2 Conn



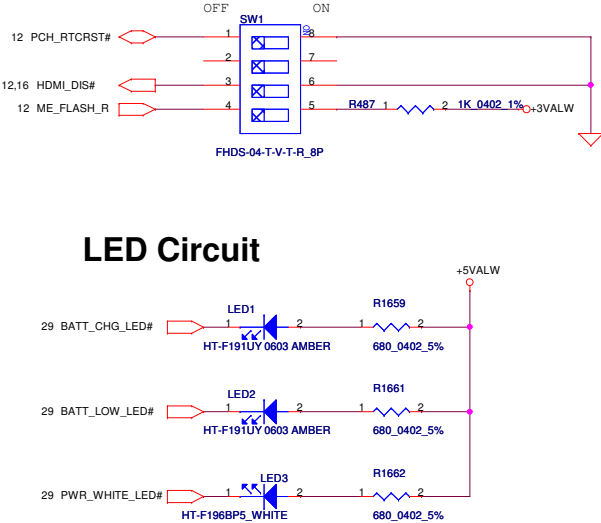
BUZZER

EC Beep

PCH Beep

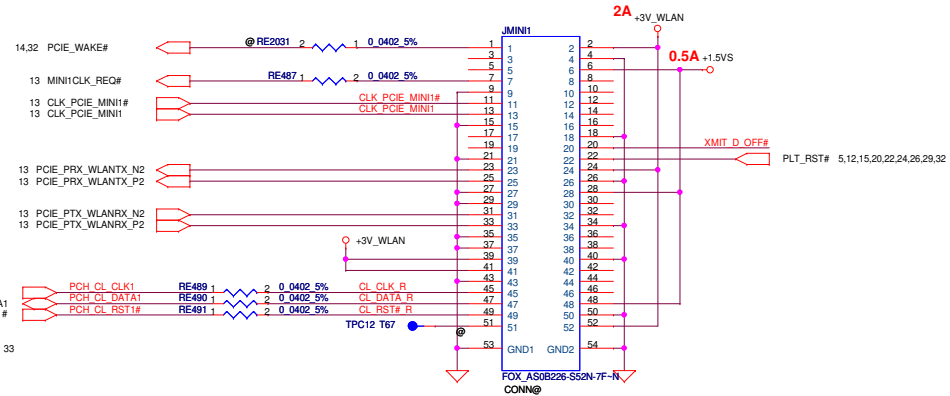


LED Circuit



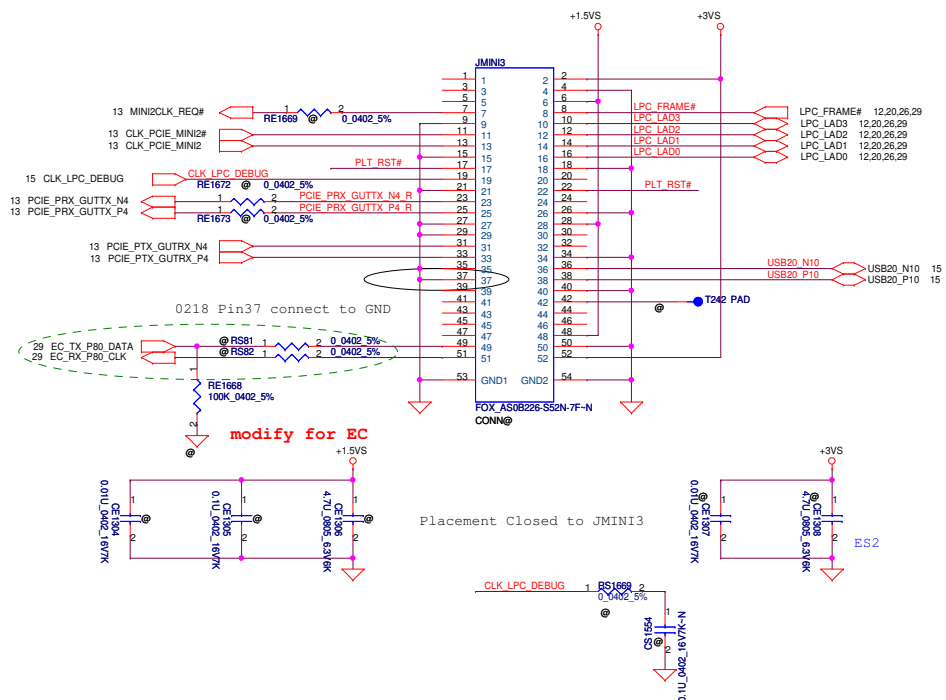
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						Size	Document Number			Rev		
							LA-6691P			0.6		
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Reserve for port80 card use for FCS in factory side.



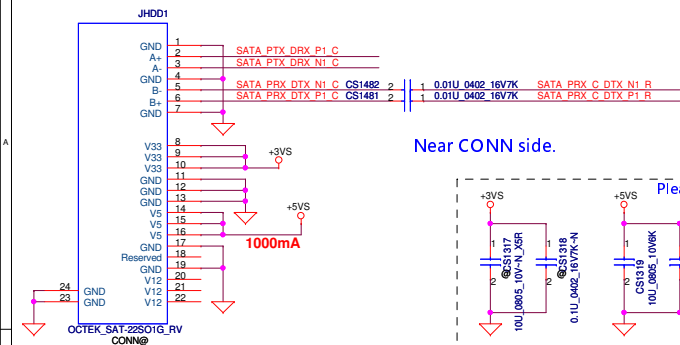
SSD(Mini Card2)

Cancel by DRD v7.0

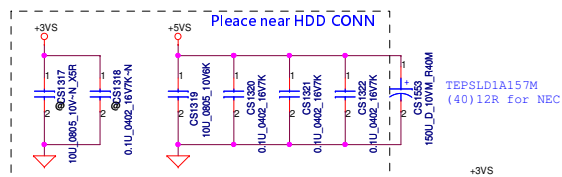


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					LA-669IP
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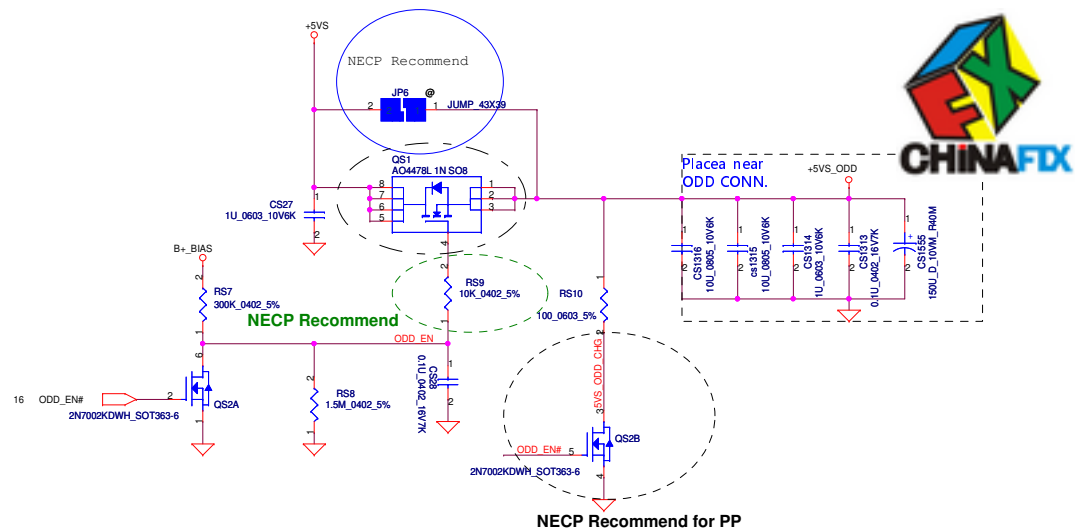
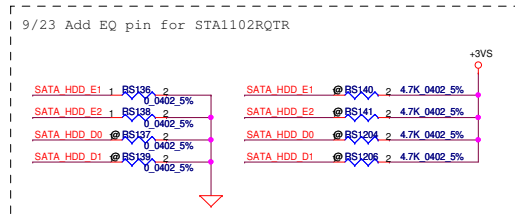
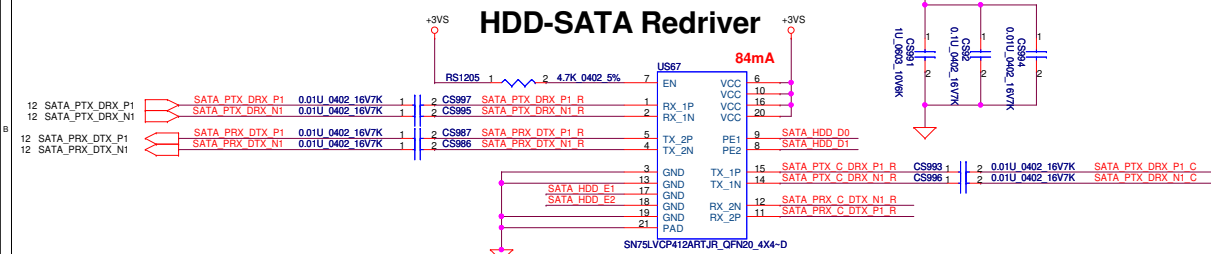
SATA HDD CONN.



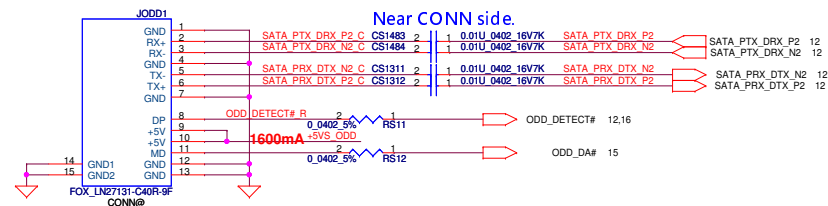
Near CONN side.



HDD-SATA Redriver



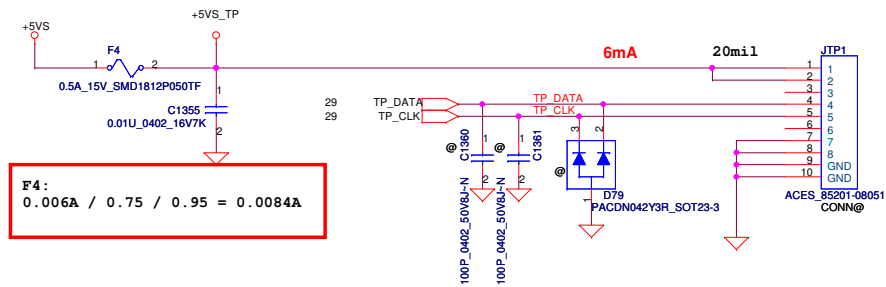
SATA ODD CONN.



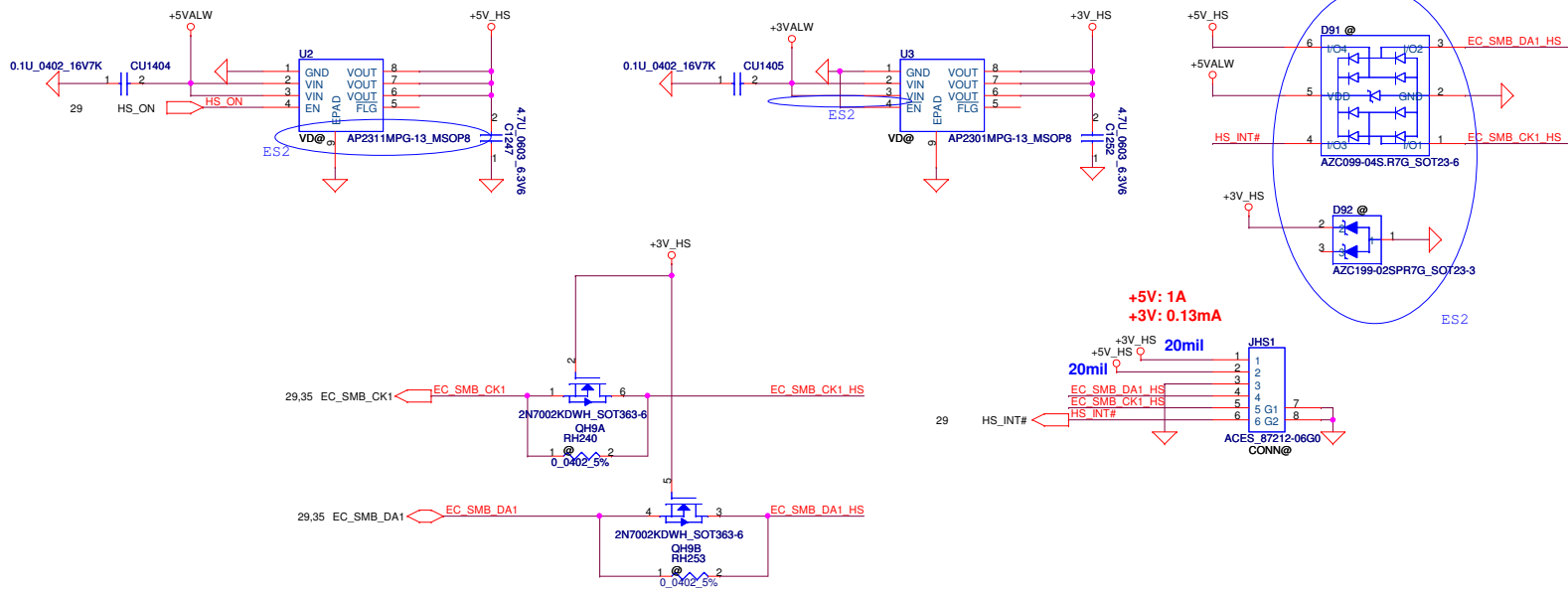
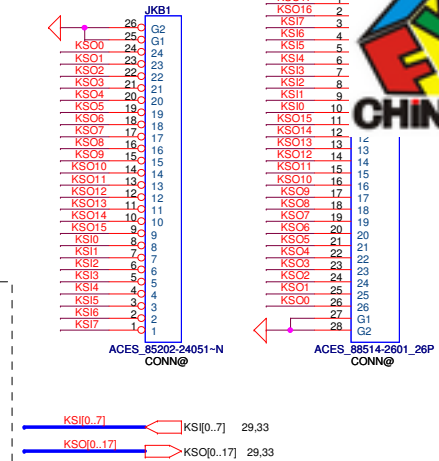
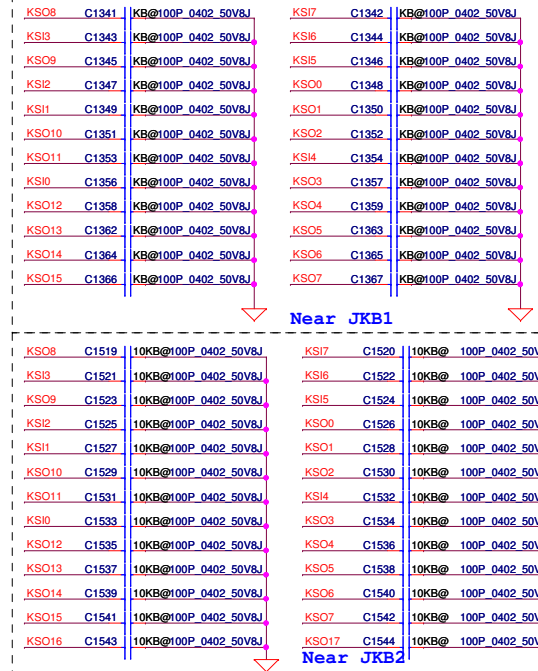
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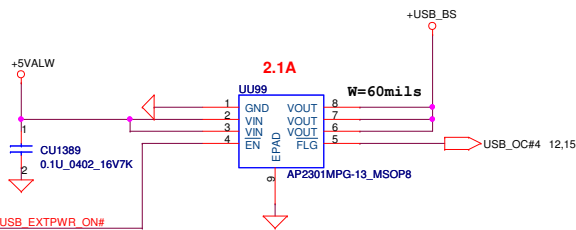
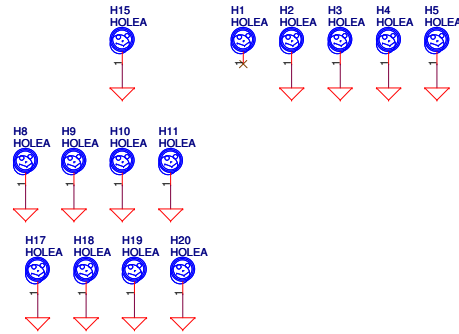
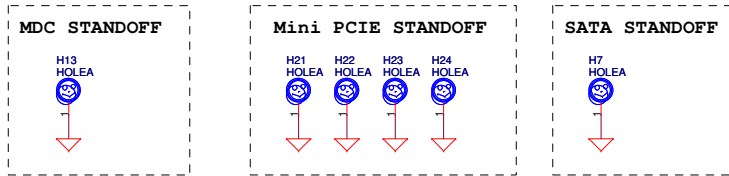
TouchPad



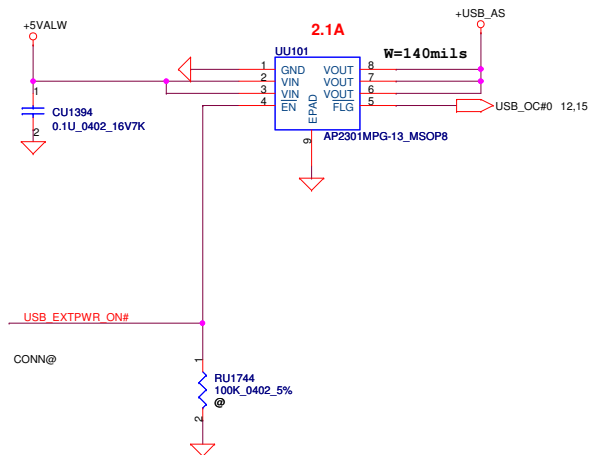
INT_KBD CONN.



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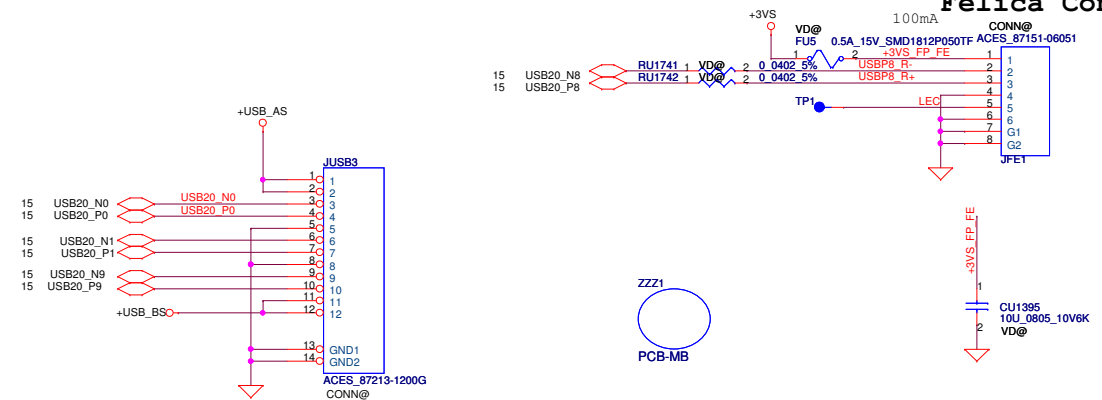


USB Sub Board CONN.



FU5:
0.1A / 0.75 / 0.95 = 0.14A

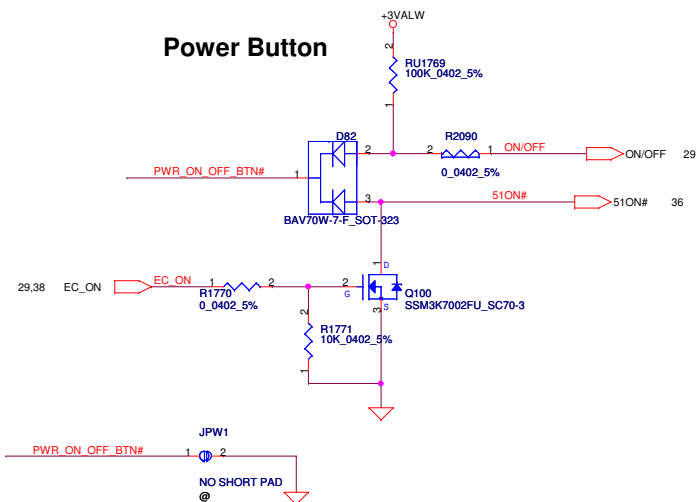
Felica Conn



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				Size	Document Number
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				Date	Friday, February 25, 2011
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				Rev	0.6

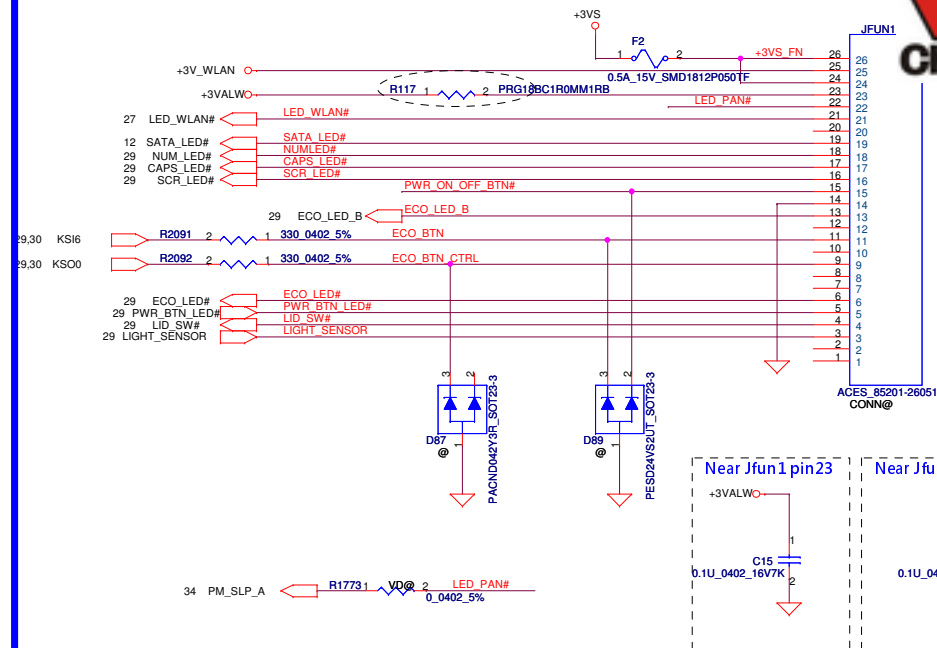


Power Button

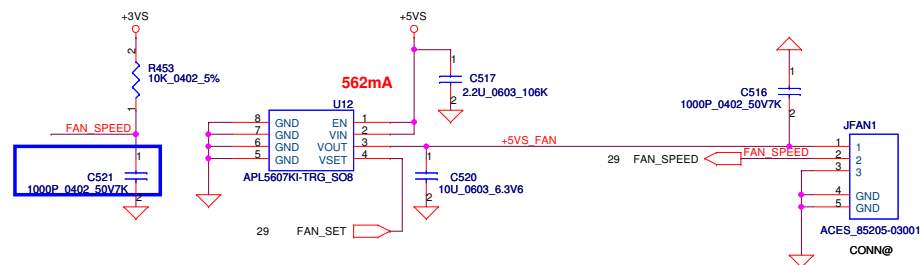


Function/B CONN.

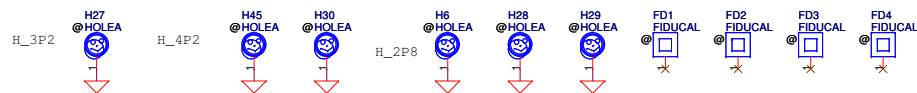
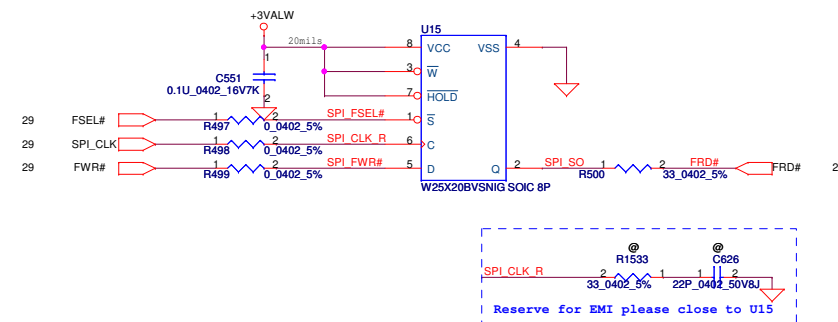
$$F2: 0.16A / 0.75 / 0.95 = 0.225A$$



Fan Control Circuit



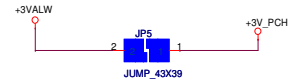
SPI ROM 256KB



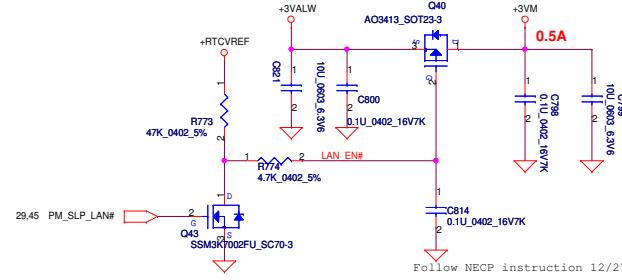
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Size				Document Number				Rev			
Custom				LA-6691P				0.6			
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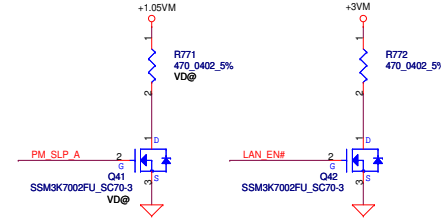
+3VALW to +3V_PCH



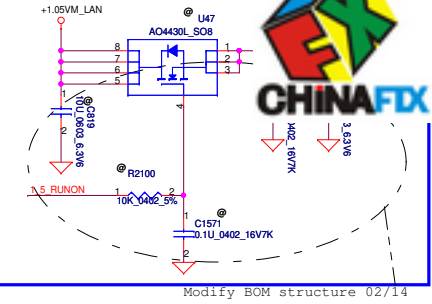
+3VALW to +3VM Transfer



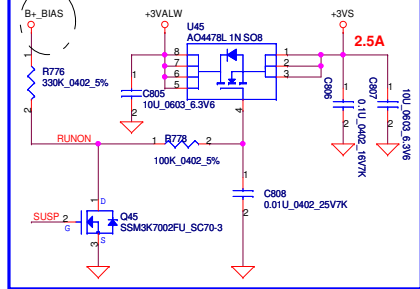
Discharge circuit-2 for V-M



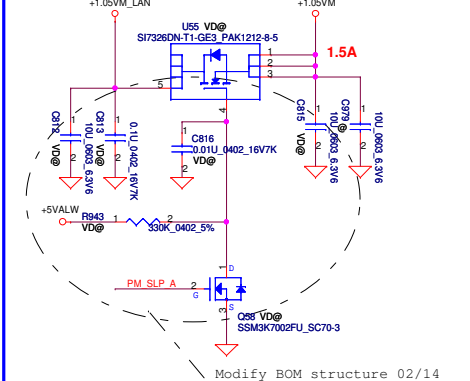
+1.05VM_LAN to +1.0



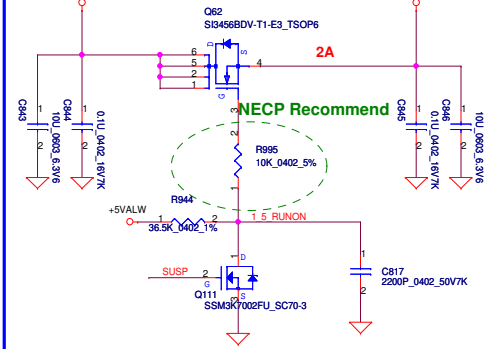
+3VALW to +3VS Transfer



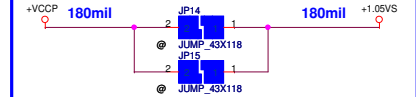
+1.05VM_LAN to +1.05VM Transfer



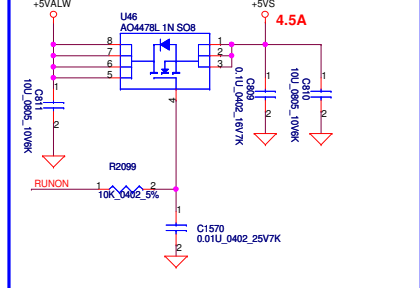
+1.5V to +1.5VS Transfer

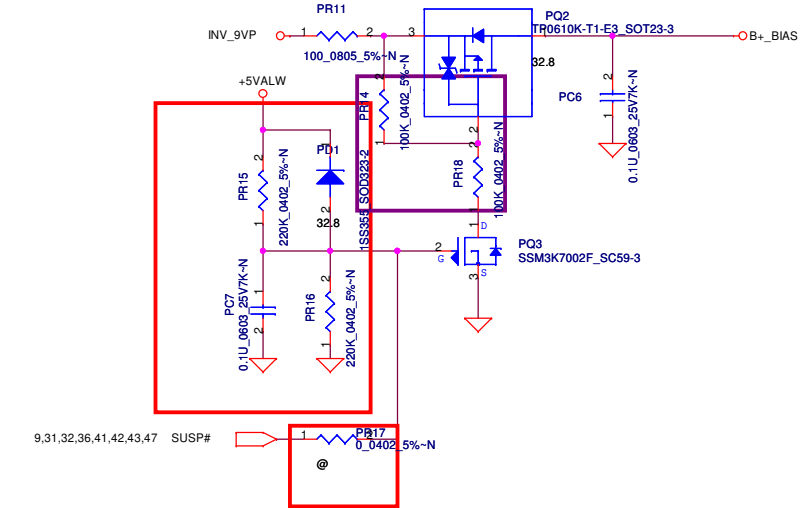
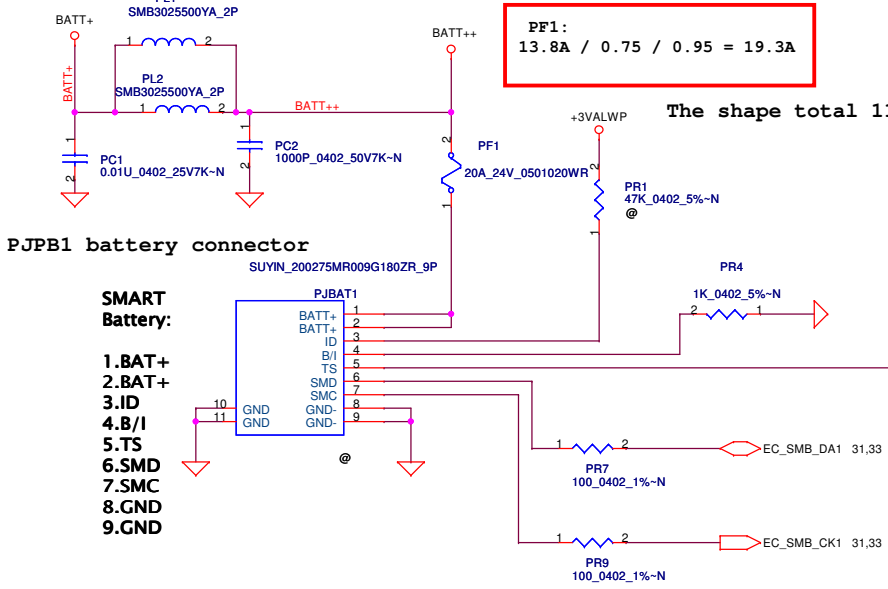


+VCCP to +1.05VS



+5VALW to +5VS Transfer

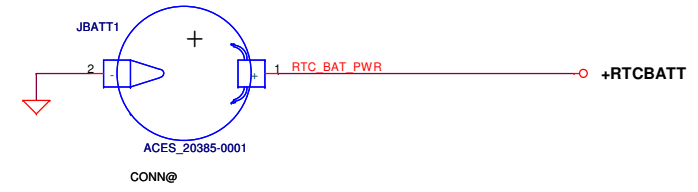
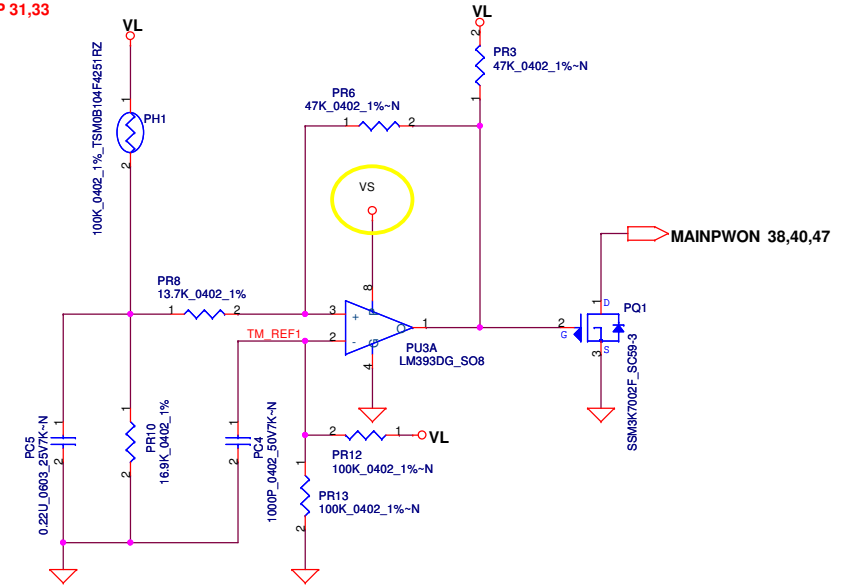




Modify 9/29

CPU OTP

PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



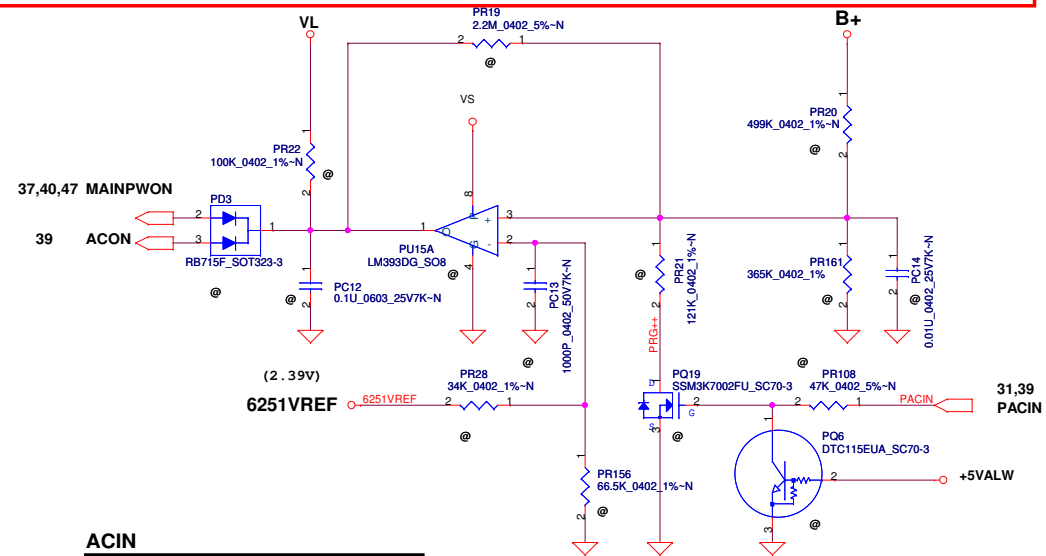
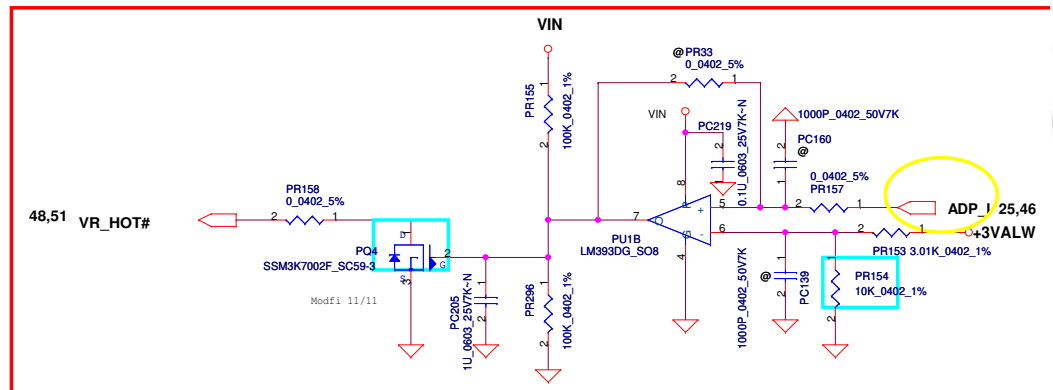
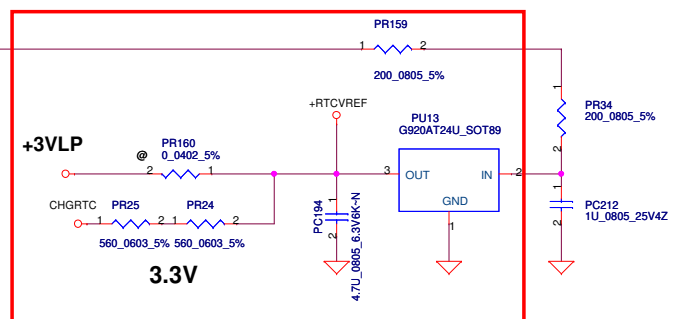
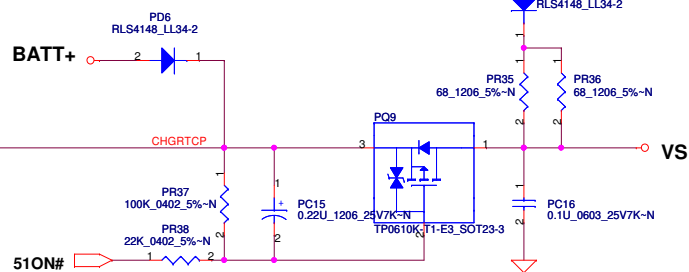
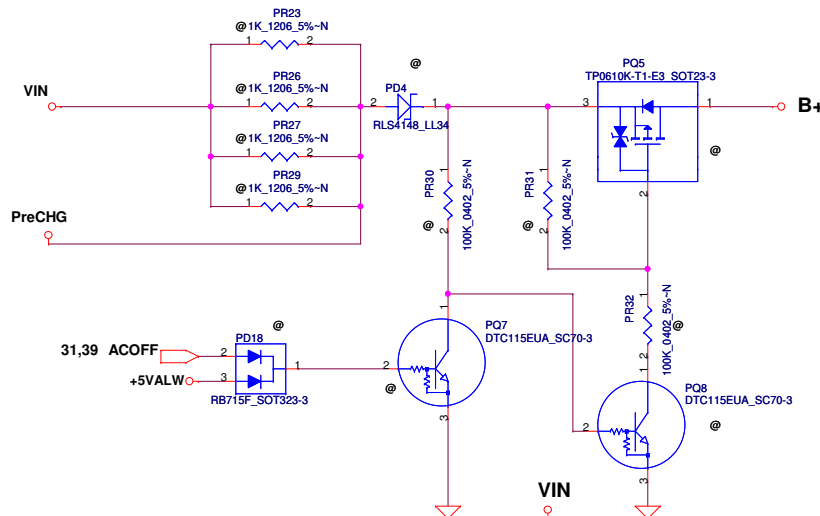
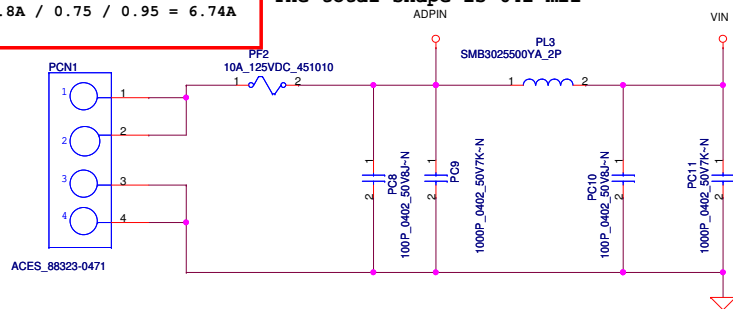
RTC Battery

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Issued Date		2010/05/05	Deciphered Date	2010/2/6		Title
				BATTERY CONN/OTP		
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PF2:
4.8A / 0.75 / 0.95 = 6.74A

The total shape is 642 mil

ADPIN



ACIN

Precharge detector			
Min.	typ.	Max.	
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

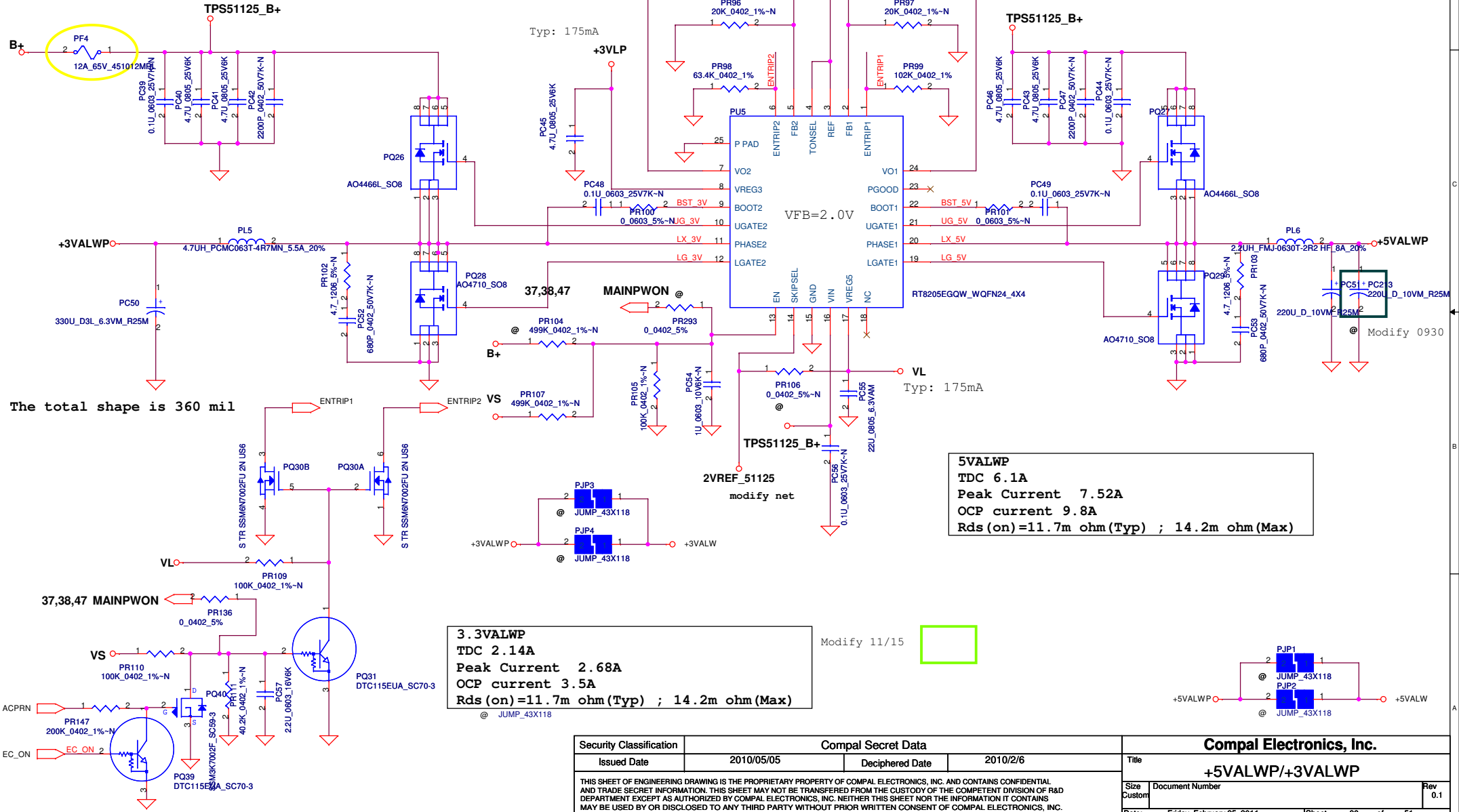
Precharge detector			
Min.	typ.	Max.	
H-->L	4.92V	6.1V	5.25V
L-->H	6.062V	6.244V	6.43V

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						Size		Document Number		Rev	
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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

PF4:
 $7.83A / 0.75 / 0.95 = 11A$

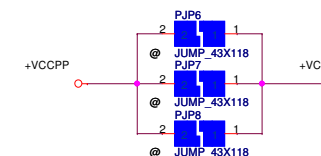
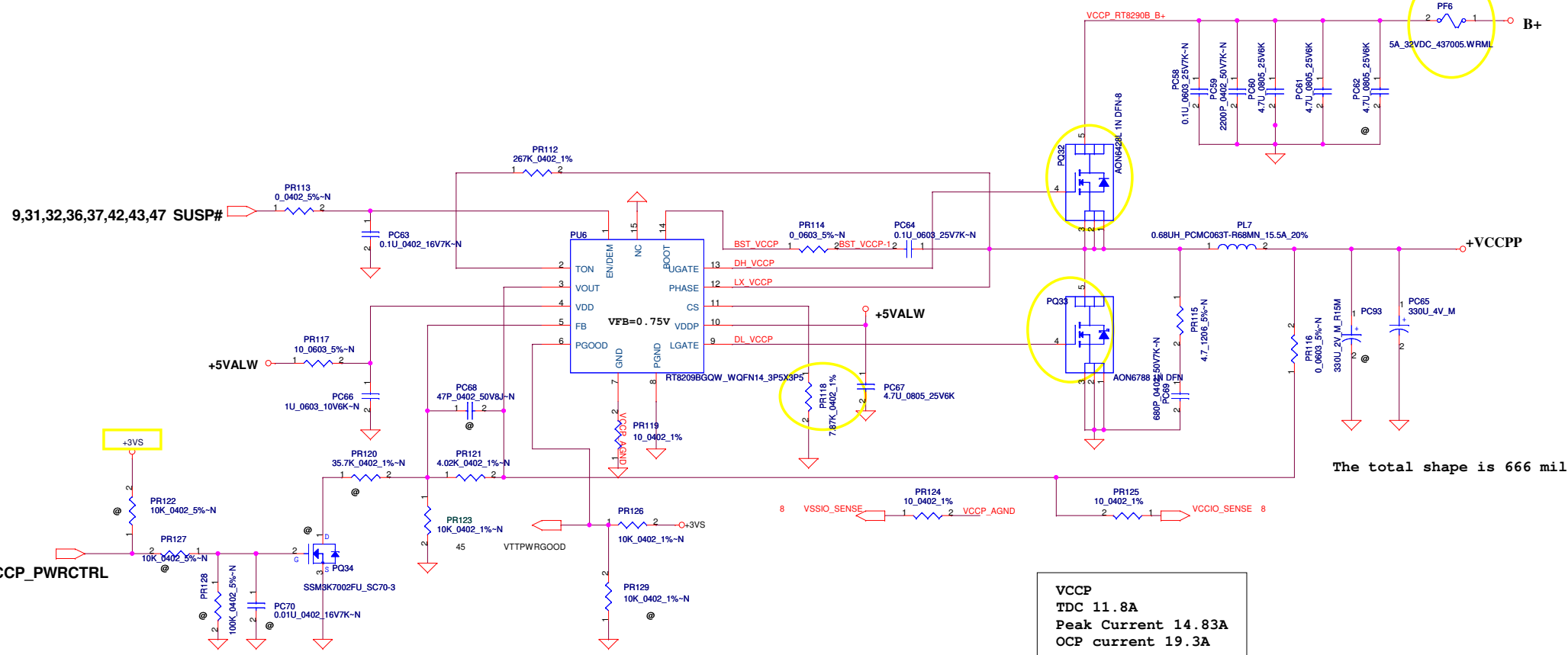
The total shape is 420 mil



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								+5VALWP/+3VALWP	
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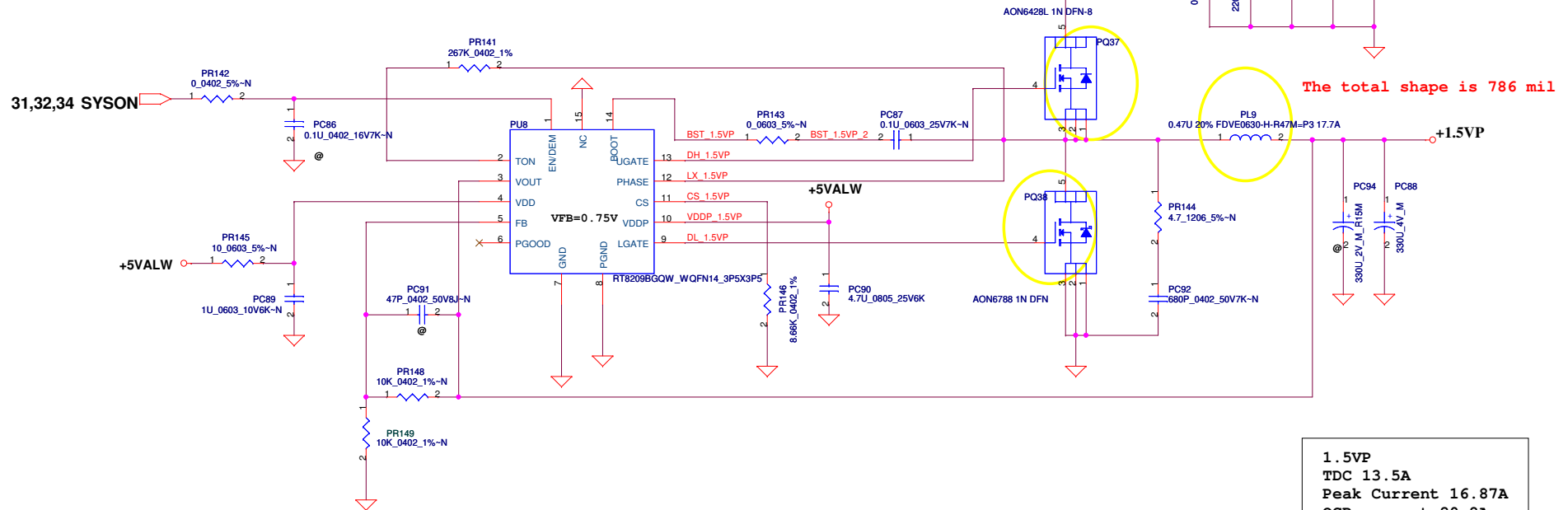
PF6:
2.59A / 0.75 / 0.95 = :

The total shape is 30U mil

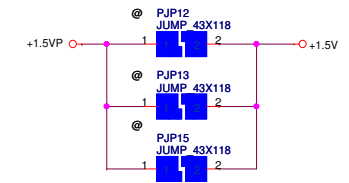
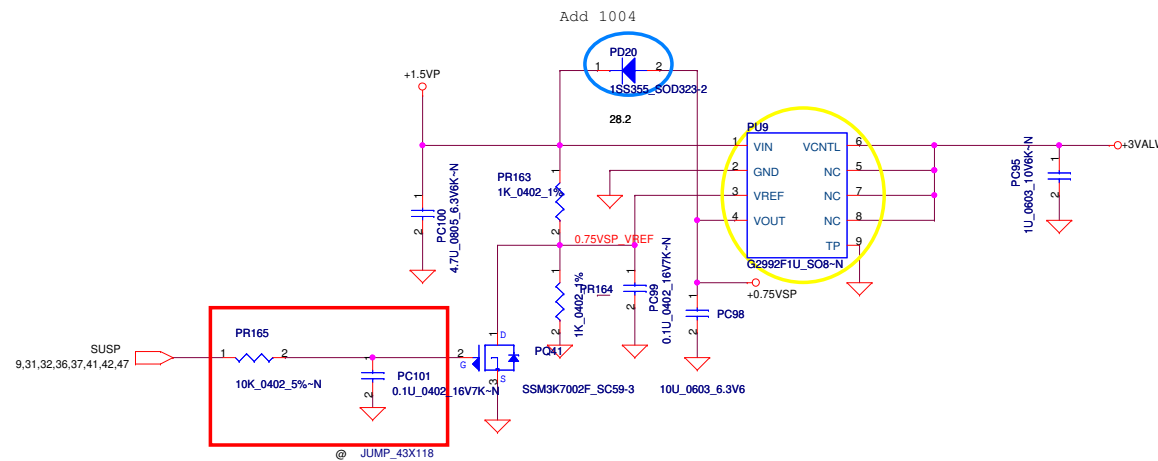


$$PF8: 4.3A / 0.75 / 0.95 = 6.1A$$

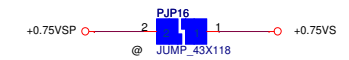
The total shape is 84 mil



1.5VP
TDC 13.5A
Peak Current 16.87A
OCP current 20.8A

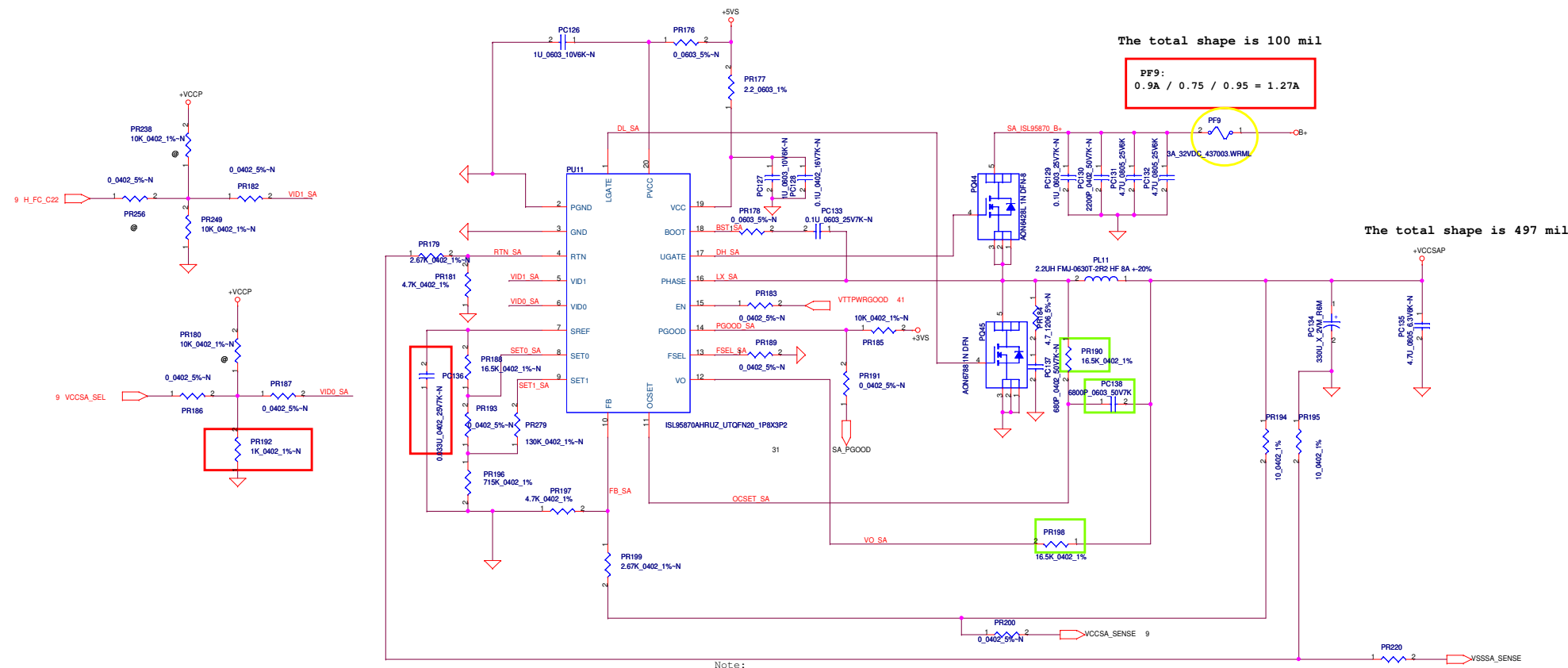


0.75VSP
TDC 1A
Peak Current 2A
OCP current 3A



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				Deciphered Date				+1.5VSP/0.75VSP			
				2008/6/05				Size			
								Document Number			
								Custom			
								Rev			
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The total shape is 100 mil

PF9:
0.9A / 0.75 / 0.95 = 1.27A

The total shape is 497 mil

Note:
RTN pin need reference output GND

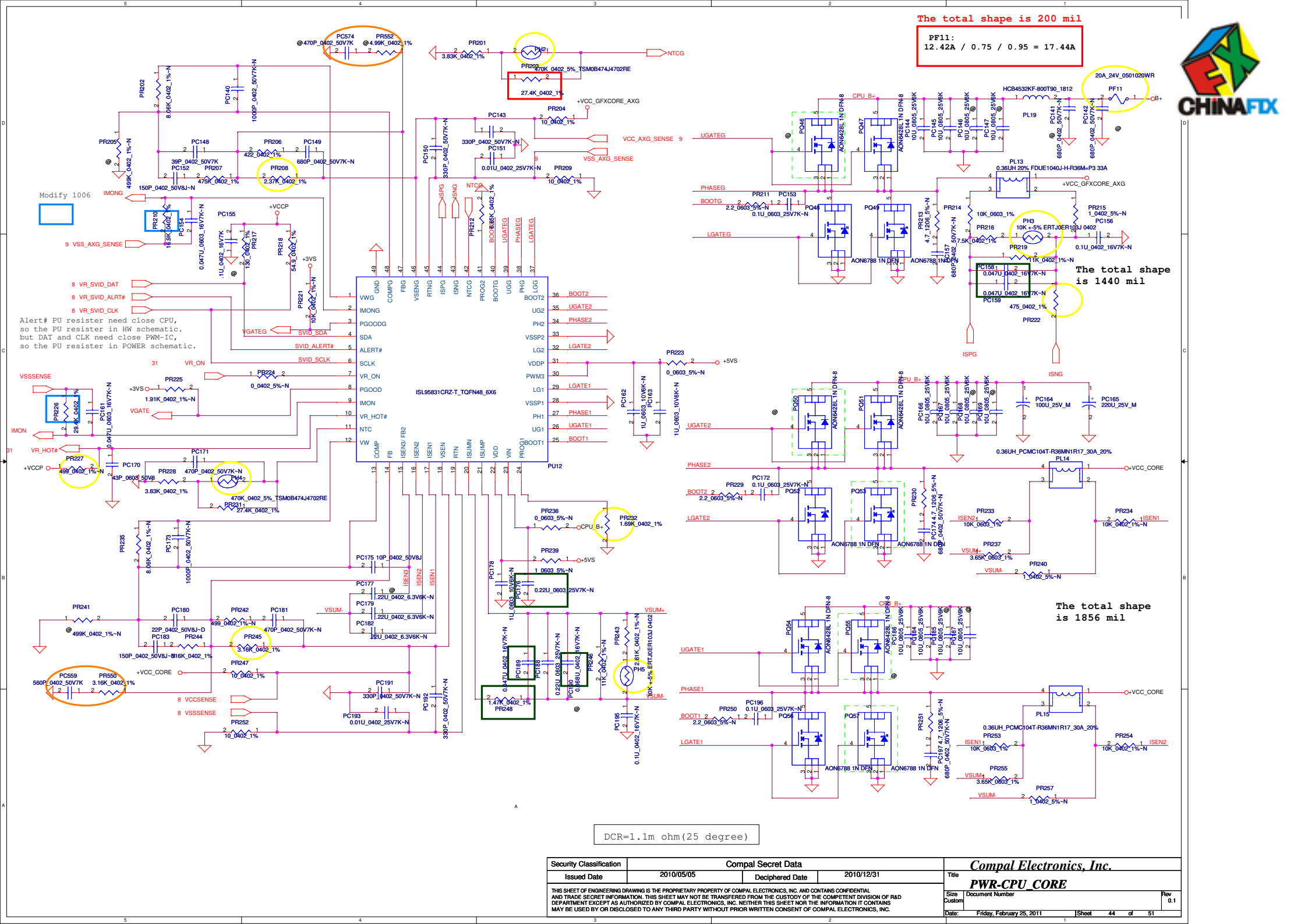
VID[0]	VID[1]	VCCSA Vout	Required	Require on 2012
0	0	0.9V	Yes	Yes
0	1	0.8V	Yes	Yes
1	0	0.75V	NO	Yes
1	1	0.65V	NO	Yes

+VCCSAP
TDC 4.8A
Peak Current 6A
OCP current 8A



Modify 11/21

Modify 11/15

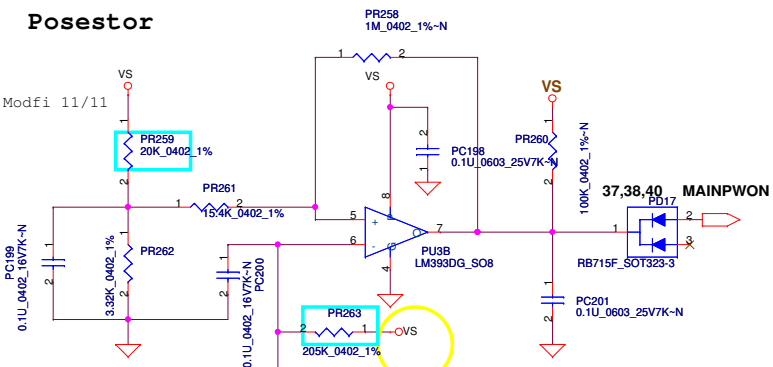


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Posesor



Modfi 11/11



The total shape
is 105 mil

$$PF10: 0.217A / 0.75 / 0.95 = 0.3A$$

Del PR269

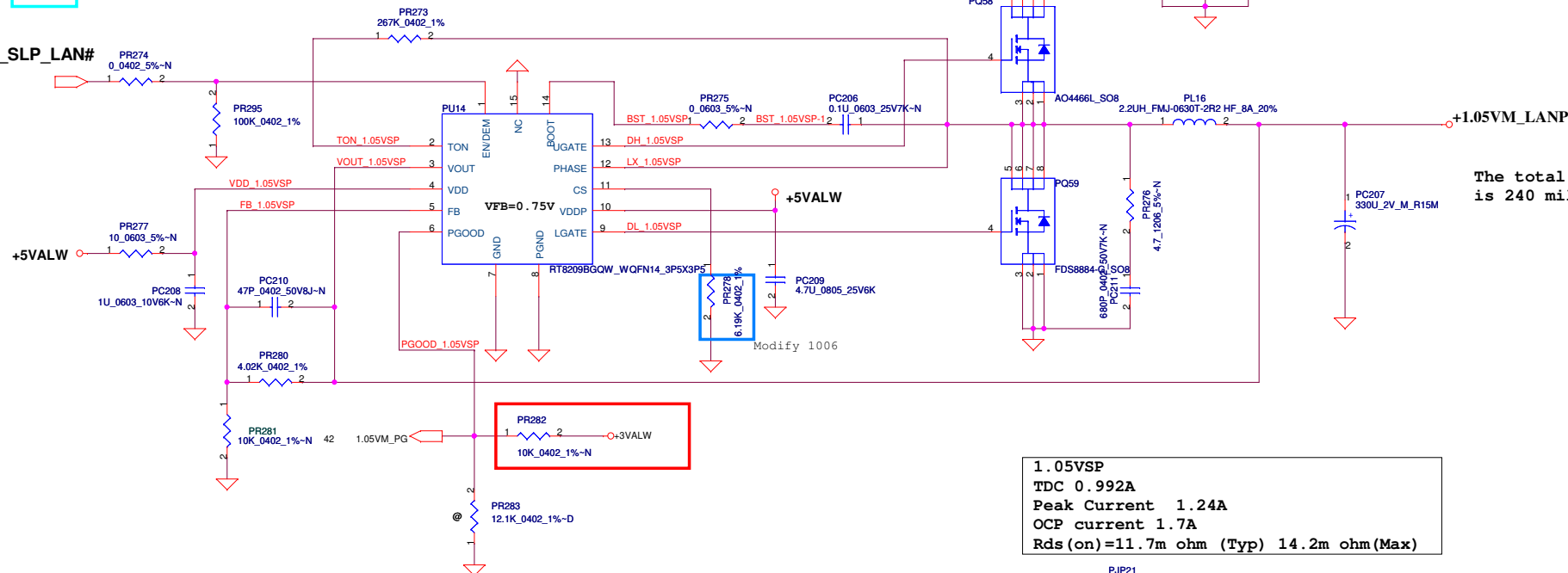
Modify 9/29

HW Parts

Modfi 11/11

PM_SLP_LAN#

6,37,41,42,43



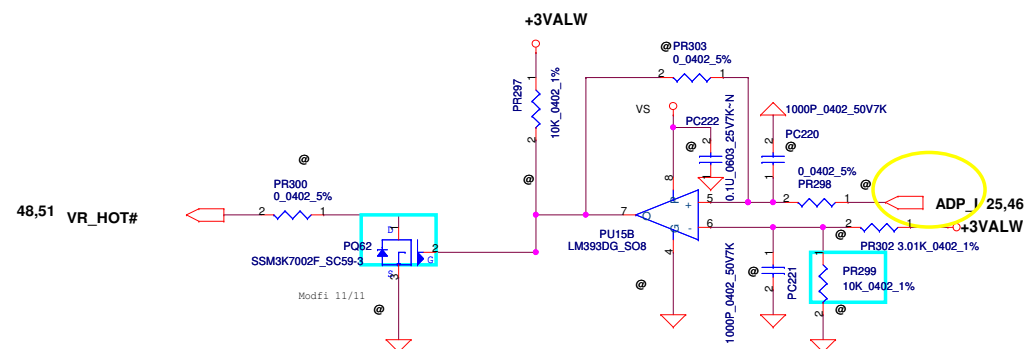
The total shape
is 240 mil

1.05VSP
TDC 0.992A
Peak Current 1.24A
OCP current 1.7A
Rds(on)=11.7m ohm (Typ) 14.2m ohm(Max)



@ JUMP_43X118

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Version Change List (P. I. R. List)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Re
1	37	BATTERY CONN/OTP	10' 06/25	Compal_Roger	For power sequence	Add(SD028220380 S RES 1/16W 220K +-5% 0402) Location : PR15, PR16	
2	37	BATTERY CONN/OTP	10' 06/25	Compal_Roger	For power sequence	Add(SC1S3355003 S DIO 1S3355) Location : PD1	
3	37	BATTERY CONN/OTP	10' 06/25	Compal_Roger	For power sequence	Add(SE042104KN0 S CER CAP .1U 25V K X7R 0603) Location : PC7	
4	37	BATTERY CONN/OTP	10' 06/25	Compal_Roger	For power sequence	DEL(SD028000080 S RES 1/16W 0 +-5% 0402) Location : PR17	
5	43	0.75VSP	10' 06/25	Compal_Roger	For S3 request	Add(SD034100280 S RES 1/16W 10K +-1% 0402) Location : PR165	
6	43	0.75VSP	10' 06/25	Compal_Roger	For S3 request	Add(SE076104KN0 S CER CAP .1U 16V K X7R 0402) Location : PC101	
7	46	CPU_CORE	10' 06/25	Compal_Roger	For cost down	Change(SD00000H280 S RES 1/10W 27.4K +-0.1% 0603) to (SD034274280 S RES 1/16W 27.4K +-1% 0402) Location : PR203	
8	47	1.05VSP	10' 06/25	Compal_Roger	For 1.05VM_PAN power good	Add(SD034100280 S RES 1/16W 10K +-1% 0402) Location : PR282	
9	46	CPU_CORE	10' 06/25	Compal_Roger	VCC_AXG transient compensation	Change(SL200000F80 S THERM_ 6.8K +-5% TSM1A682J4302RE) to (SL200000200 S THERM_ 10K +-5% ERTJ1VR103J 0603) Location : PH3	
10	47	1.05VSP	10' 06/25	Compal_Roger	For power sequence	Change 1.05VM power good pull high from +3VS to +3VALW	
11	39	Charger	10' 07/05	Compal_Roger	Prevent back to back mos damage	Change(SB00000DL00 S TR A04407A 1P S08) to (SB00000I600 S TR SI4459ADY-T1-GE3 1P S08) Location : PQ11	
12	39	Charger	10' 07/05	Compal_Roger	Prevent back to back mos damage	Add(SE075562K80 S CER CAP 5600P 25V K X7R 0402) Location : PC96	
13	39	Charger	10' 07/06	Compal_Roger	Reduce charger ripple voltage	Add(SE00000QKN0 S CER CAP 10U 25V K X5R 0805 H1.25) Location : PC97,PC103	
14	46	CPU_CORE	10' 07/29	Compal_Roger	For AXG loadline	Change(SD034237180 S RES 1/16W 2.37K +-1% 0402) to (SD000004080 S RES 1/16W 2.2K +-1% 0402) Location : PR208	
15	46	CPU_CORE	10' 07/29	Compal_Roger	For CPU OCP setting point	Change(SD034909080 S RES 1/16W 909 +-1% 0402) to (SD000009480 S RES 1/16W 1.47K +-1% 0402) Location : PR248	
16	46	CPU_CORE	10' 07/29	Compal_Roger	For voltage rating	Change(SE080224KN0 S CER CAP .22U 10V K X7R 0603) to (SE0000052N0 S CER CAP 0.22U 25V K X7R 0603) Location : PC176	
17	46	CPU_CORE	10' 07/29	Compal_Roger	For CPU transient	Change(SE000003JN0 S CER CAP 0.068U 16V K X7R 0402) to (SE076473KN0 S CER CAP .047U 16V K X7R 0402) Location : PC189	
18	46	CPU_CORE	10' 07/29	Compal_Roger	For CPU transient	Delete(SE000003JN0 S CER CAP 0.068U 16V K X7R 0402) Location : PC190	
19	46	CPU_CORE Location : PC158	10' 07/29	Compal_Roger	For AXG transient	Change(SE076104KN0 S CER CAP .1U 16V K X7R 0402) to (SE076473KN0 S CER CAP .047U 16V K X7R 0402)	

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Re
20	44	CPU_CORE	10' 07/29	Compal_Roger	For AXG transient	Change (SE0751032N0 S CER CAP .01U 25V K X7R 0402) to (SE076473KN0 S CER CAP .047U 16V K X7R 0402) Location : PC159	
21	44	CPU_CORE	10' 07/29	Compal_Roger	For AXG OCP	Change (SD034549080 S RES 1/16W 549 +-1% 0402) to (SD00000EL80 S RES 1/16W 487 +-1% 0402) Location : PR222	
22	37	Charger	10' 08/26	Compal_Roger	Prevent ACIN droop when plug out battery with AC	Change (SD00000QM80 S RES 1/16W 14.3K +-1% 0402) to (SD034169280 S RES 1/16W 16.9K +-1% 0402) Location :PR49	
23	44	CPU_CORE	10' 08/26	Compal_Roger	For turbo mode request	Add (SD034499080 S RES 1/16W 499 +-1% 0402) Location :PR227	
24	44	CPU_CORE	10' 08/26	Compal_Roger	For turbo mode setting	Change (SD034787180 S RES 1/16W 7.87K +-1% 0402) to (SD00000J280 S RES 1/16W 4.32K +-1% 0402) Location :PR232	
25	44	CPU_CORE	10' 08/26	Compal_Roger	For AXG OCP setting	Change (SD00000EL80 S RES 1/16W 487 +-1% 0402) to (SD00000C080 S RES 1/16W 590 +-1% 0402) Location :PR222	
26	44	CPU_CORE	10' 08/26	Compal_Roger	For AXG Loadline setting	Change (SD000004080 S RES 1/16W 2.2K +-1% 0402) to (SD034237180 S RES 1/16W 2.37K +-1% 0402) Location :PR208	
27	44	CPU_CORE	10' 08/26	Compal_Roger	For CPU loadline setting	Change (SD014205180 S RES 1/10W 2.05K +-1% 0603) to (SD014316180 S RES 1/10W 3.16K +-1% 0603) Location :PR245	
28	44	CPU_CORE	10' 08/26	Compal_Roger	For Cost down	Change (SL200000200 S THERM_ 10K +-5% ERTJ1VR103J 0603) to (SL200001100 S THERM_ 10K +-5% ERTJ0ER103J 0402) Location :PH3,PH5	
29	44	CPU_CORE	10' 08/26	Compal_Roger	For Cost down	Change (SL200000880 S THERM_ 470K J NCP18WM474J03RB 0603) to (SL200000J00 S THERM_ 470K +-5% TSM0B474J4702RE 0402) Location :PH2,PH4	
30	44	CPU_CORE	10' 08/31	Compal_Roger	For AXG rating	Change (SH000005680 S COIL 0.36UH +-20% PCMC104T-R36MNI17) to (SH00000HQ00 S COIL .36UH 20% FDUE1040J-H-R36M-P3 33A) Location :PL13	
31	44	CPU_CORE	10' 09/1	Compal_Roger	For Compal common Design	Change (SB00000K300 S TR SIR472DP-T1-GE3 1N POWERPAK S08) to (SB00000J200 S TR AON6428L 1N DFN-8) Location :PQ46,PQ47,PQ50,PQ51,PQ54,PQ55	
32	44	CPU_CORE	10' 09/1	Compal_Roger	For Compal common Design	Change (SB00000I900 S TR AON6704L 1N DFN) to (SB00000P300 S TR AON6788 1N DFN) Location :PQ48,PQ49,PQ52,PQ53,PQ56,PQ57	
33	35	BATTERY CONN/OTP	10' 09/1	Compal_Roger	For RTC battery charge	Del (SCS00000Z00 S SCH DIO RB751V-40 SOD-323) Location :PD2	
34	39/41	1.5VP/VCCPP	10' 09/1	Compal_Roger	For Compal common Design	Change (SB00000K300 S TR SIR472DP-T1-GE3 1N POWERPAK S08) to (SB00000J200 S TR AON6428L 1N DFN-8) Location :PQ32,PQ37	
35	39/41	1.5VP/VCCPP	10' 09/1	Compal_Roger	For Compal common Design	Change (SB00000I900 S TR AON6704L 1N DFN) to (SB00000P300 S TR AON6788 1N DFN) Location :PQ33,PQ38	
36	39/41	1.5VP/VCCPP	10' 09/1	Compal_Roger	For 1.5V and VCCP OCP setting	Change (SD000002680 S RES 1/16W 6.98K +-1% 0402) to (SD028102280 S RES 1/16W 10.2K +-1% 0402) Location :PR146,PR118	
37	36	DC IN 40P6T0R PC159,PC160,PC194,PC212	10' 09/1	Compal_Roger	For RTC battery and turbo mode request	ADD PR33,PR34,PR153,PR154,PR155,PR156,PR157,PR158,PR159,	

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38	41	0.75VSP	10' 09/24	Compal_Roger	Compal Internal request	Change (SA053310110 S IC APL533HKAC-TRL SOP-8-P 8P LDO) to (SA00000VE80 S IC G2992FIU SO 8P 0.9V) Location :PU9	
39	36	DCIN/DETECTOR	10' 09/24	Compal_Roger	RTC battery charge	Add PR24,PR25(560 ohm 0603)	
40	37	CHARGER	10' 09/24	Compal_Roger	Batt_OVP setting	Change (SD034121380 S RES 1/16W 121K +-1% 0402) to (SD034118380 S RES 1/16W 118K +-1% 0402) Location :PR93	
41	37	CHARGER	10' 09/24	Compal_Roger	Fuse derating	Change (SP04107P030 S FUSE 429007.WRML 7A 24V UL/CSA FAST) to (SP040002K00 S FUSE 0437005.WR 5A 32V UL FAST) Location :PF3	
42	45	1.05VM	10' 09/24	Compal_Roger	For cost down	Change (SL200000S00 S THERM_470 +-50% PRF18BA471QB5RB 0603) to (SL2000001F00 S THERM_1K +-50% PRF15BA102RB6RC 0402) Location :PR264, PR265, PR266, PR267, PR268, PR269, PR270, PR271, PR272, PR284, PR285, PR286, PR287, PR288, PR289	
43	42	INV_9V	10' 09/24	Compal_Roger	For cost down	Change (SC11Q804000 S DiO EC31Q504 5X2.5) to (SCS00000W00 S SCH DIO SX34 SMA) Location :PD15,PD16	
44	38	3VALWP/5VALWP	10' 09/24	Compal_Roger	Fuse derating	Change (SP04107P030 S FUSE 429007.WRML 7A 24V UL/CSA FAST) to (SP04110P010 S FUSE 12A 65V UL/CSA FAST) Location :PF4	
45	37	CHARGER	10' 09/24	Compal_Roger	Sourcer request	Change (SB000001600 S TR SI4459ADY-T1-GE3 1P S08) to (SB00000JD10 S TR AO4409L 1P S08) Location :PQ11,PQ13	
46	39	VCCPP	10' 09/24	Compal_Roger	Fuse derating	Change (SP04107P030 S FUSE 429007.WRML 7A 24V UL/CSA FAST) to (SP040002L00 S FUSE 0437003.WR 3A 32V UL FAST) Location :PF6	
47	37	CHARGER	10' 09/24	Compal_Roger	For leakage issue	Add PD19	
48	40	1.8VSP	10' 09/24	Compal_Roger	Fuse derating	Change (SP04107P030 S FUSE 429007.WRML 7A 24V UL/CSA FAST) to (SP040003300 S FUSE 0437001.WR 1A 63V UL/CSA FAST) Location :PF7	
49	37	CHARGER	10' 09/24	Compal_Roger	Fuse derating	Change (SH000005K80 S COIL .68UH +-20% PCMC063T-R68MN 15.5A) to (SH00000GQ00 S COIL .47U 20% FDVE0630-H-R47M=P3 17.7A) Location :PL7	
50	42	INV_9V	10' 09/24	Compal_Roger	Fuse derating	Change (SP04107P030 S FUSE 429007.WRML 7A 24V UL/CSA FAST) to (SP040002K00 S FUSE 0437005.WR 5A 32V UL FAST) Location :PF5	
51	43	VCCSAP	10' 09/24	Compal_Roger	Fuse derating	Change (SP04107P030 S FUSE 429007.WRML 7A 24V UL/CSA FAST) to (SP040002L00 S FUSE 0437003.WR 3A 32V UL FAST) Location :PF9	
52	44	CPU_CORE	10' 09/24	Compal_Roger	Fuse derating	Change (SP040000M00 S FUSE 451008MRL 8A 125V UL/CSA FAST) to (SP040001N00 S FUSE 0501020WR 20A 24V UL/CSA FAST) Location :PF11	
53	45	1.05VM	10' 09/24	Compal_Roger	Fuse derating	Change (SP04107P030 S FUSE 429007.WRML 7A 24V UL/CSA FAST) to (SP040002L00 S FUSE 0437003.WR 3A 32V UL FAST) Location :PF10	
54	35	BATTERY CONN/OTP	10' 09/29	Compal_Roger	NECP request	Change (SD028470380 S RES 1/16W 470K +-5% 0402) to (SD028100380 S RES 1/16W 100K +-5% 0402) Location :PR14	
55	35/38	BATTERY CONN/OTP 3VALWP/5VALWP	10' 09/29	Compal_Roger	NECP request	ADD PR18,PC213	
56	41	0.75VSP	10' 10/04	Compal_Roger	NECP request	ADD PD20	
57	41	CPU_CORE Location :PR22Z	10' 10/06	Compal_Roger	AXG OCP setting	Change (SD00000C080 S RES 1/16W 590 +-1% 0402) to (SD034475080 S RES 1/16W 475 +-1% 0402)	

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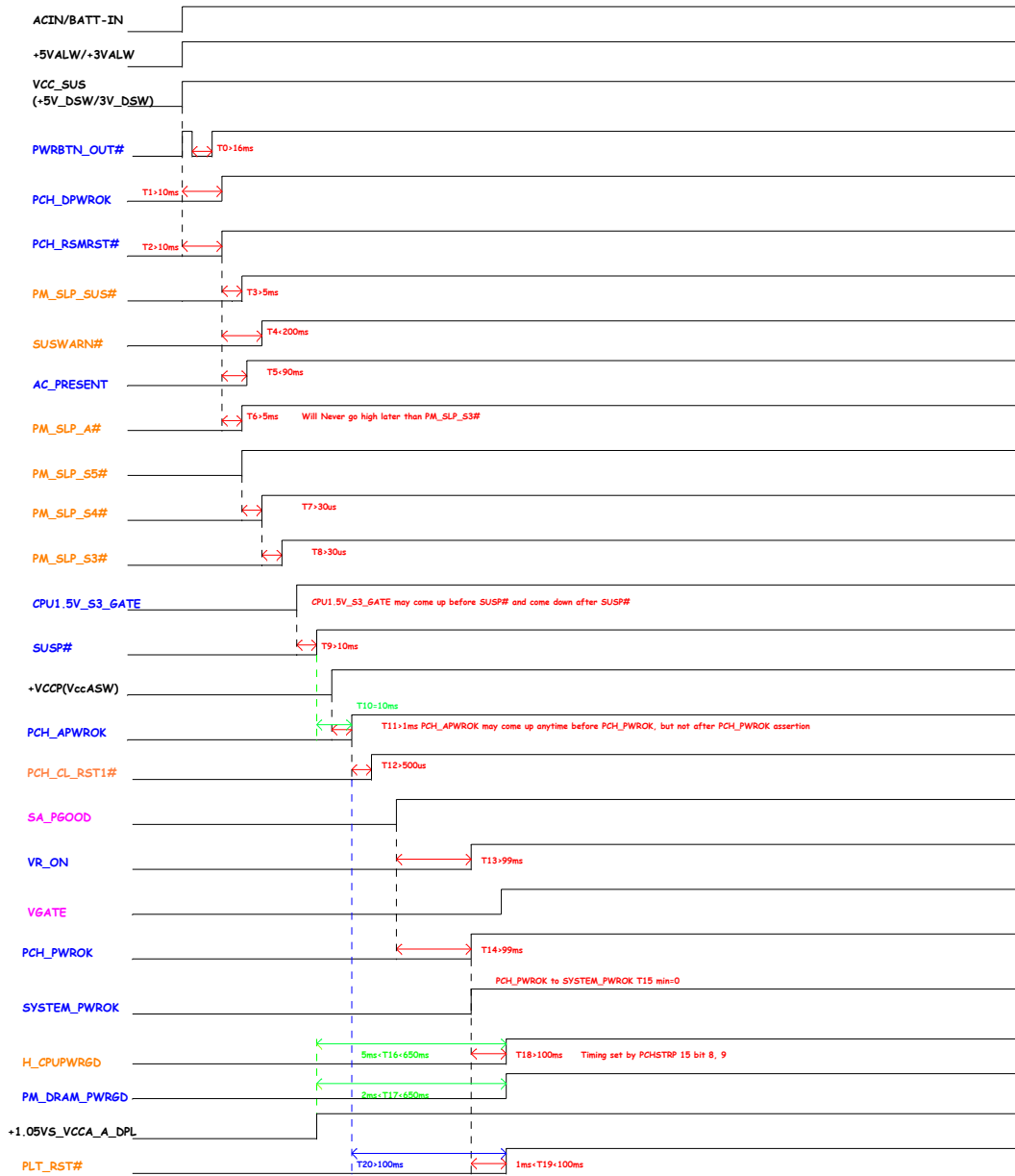


Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Re
58	44	CPU_CORE	10' 10/06	Compal_Roger	Turbo mode request	Change (SD034787180 S RES 1/16W 7.87K +-1% 0402) to (SD034169280 S RES 1/16W 16.9K +-1% 0402) Location :PR210	
59	44	CPU_CORE	10' 10/06	Compal_Roger	Turbo mode request	Change (SD034953180 S RES 1/16W 9.53K +-1% 0402) to (SD034294280 S RES 1/16W 29.4K +-1% 0402) Location :PR226	
60	45	1.05VM	10' 10/06	Compal_Roger	OCP setting	Change (SD034110280 S RES 1/16W 11K +-1% 0402) to (SD034374180 S RES 1/16W 3.74K +-1% 0402) Location :PR278	
61	40	1.8vsp	10' 10/11	Compal_Roger	Output Voltage rating	Change (SGA00000W00 S POLY C 330U 2V M LESRI5M CX H1.9) to (SGA00000Y80 S POLY C 220U 4V Y D2 ESR15M EEECX H1.9) Location :PC76	
62	45	1.05VM	10' 11/11	Compal_Roger	Posestor voltage detect	Change (SD034100280 S RES 1/16W 10K +-1% 0402) to (SD034200280 S RES 1/16W 20K +-1% 0402) Location :PR259	
63	45	1.05VM	10' 11/11	Compal_Roger	Posestor voltage detect	Change (SD034150280 S RES 1/16W 15K +-1% 0402) to (SD034205380 S RES 1/16W 205K +-1% 0402) Location :PR263	
64	37	Charger	10' 11/11	Compal_Roger	Prevent shortage issue	Change (SCIH751H010 S DIO CH751H-40PT S0D323) to (SCS00003500 S SCH DIO RB751V-40 S0D-323 YEASHIN) Location :PD8,PD13	
65	39	3VALWP/5VALWP	10' 11/15	Compal_Roger	5V OCP setting	Change (SD034196380 S RES 1/16W 196K +-1% 0402) to (SD034806280 S RES 1/16W 80.6K +-1% 0402) Location :PR99	
66	38	+VCCPP	10' 11/15	Compal_Roger	VCCP OCP setting	Change (SD028102280 S RES 1/16W 10.2K +-1% 0402) to (SD000000680 S RES 1/16W 8.45K +-1% 0402) Location :PR118	
67	40	1.8VSP	10' 11/15	Compal_Roger	1.8VSP OCP setting	Change (SD034825180 S RES 1/16W 8.25K +-1% 0402) to (SD034150180 S RES 1/16W 1.5K +-1% 0402) Location :PR135	
68	41	1.5vp	10' 11/15	Compal_Roger	1.5VP OCP setting	Change (SD028102280 S RES 1/16W 10.2K +-1% 0402) to (SD000002300 S RES 1/16W 7.68K +-1% 0402) Location :PR146	
69	43	VCCSA	10' 11/15	Compal_Roger	VCCSA OCP setting	Change (SD034316280 S RES 1/16W 31.6K +-1% 0402) to (SD034165280 S RES 1/16W 16.5K +-1% 0402) Location :PR190,PR198	
70	43	VCCSA	10' 11/15	Compal_Roger	VCCSA OCP setting	Change (SE026103KN0 S CER CAP .01U 16V K X7R 0603) to (SE025682KN0 S CER CAP 6800P 50V K X7R 0603) Location :PC138	
71	36	DCIN/detect	10' 11/19	Compal_Toby	Charger OVP active cut out the AC power	ADD (SE025682KN0 S CER CAP 6800P 50V K X7R 0603) Location :PC138	
72	37	Charger	10' 11/19	Compal_Toby	PC215 PC216 to adjust the delay time	ADD (S CER CAP .1U 25V K X7R 0603) Location :PC215 ADD (S CER CAP .1U 25V K X7R 0603) Location :PC216	
73	43	VCCSA	10' 11/21	Compal_Toby	Adjust VCCSA slew rate	Change (0.068uF) to (0.033uF) Location :PC136	
74	37	Charger	10' 11/21	Compal_Toby	Charger_OVP latch circuitry	ADD (S RES 1/16W 10K +-1% 0402)Location:PR292 ADD (S CER CAP .1U 25V K X7R 0603)Location:PC217 ADD (S TR SSM3K7002P 1N SC59-3)Location:PQ42	
75	44	CPU_CORE	11' 01/12	Compal_Roger	MOS derating	Del PQ46,PQ50,PQ55,PQ53,PQ57	0.5
76	44	CPU_CORE	11' 01/13	Compal_Roger	GFX_ICC MAX setting	Change (0 ohm) to (6.65k ohm) Location :PR212	0.5
77	40/45	1.8VSP/1.05VM Location :PQ36,PQ59	11' 01/13	Compal_Roger	RT8209 has threshold voltage to set OCP, due to senese Rds(on) ,	Change (A04710) to (FDS8884)	0.5

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Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

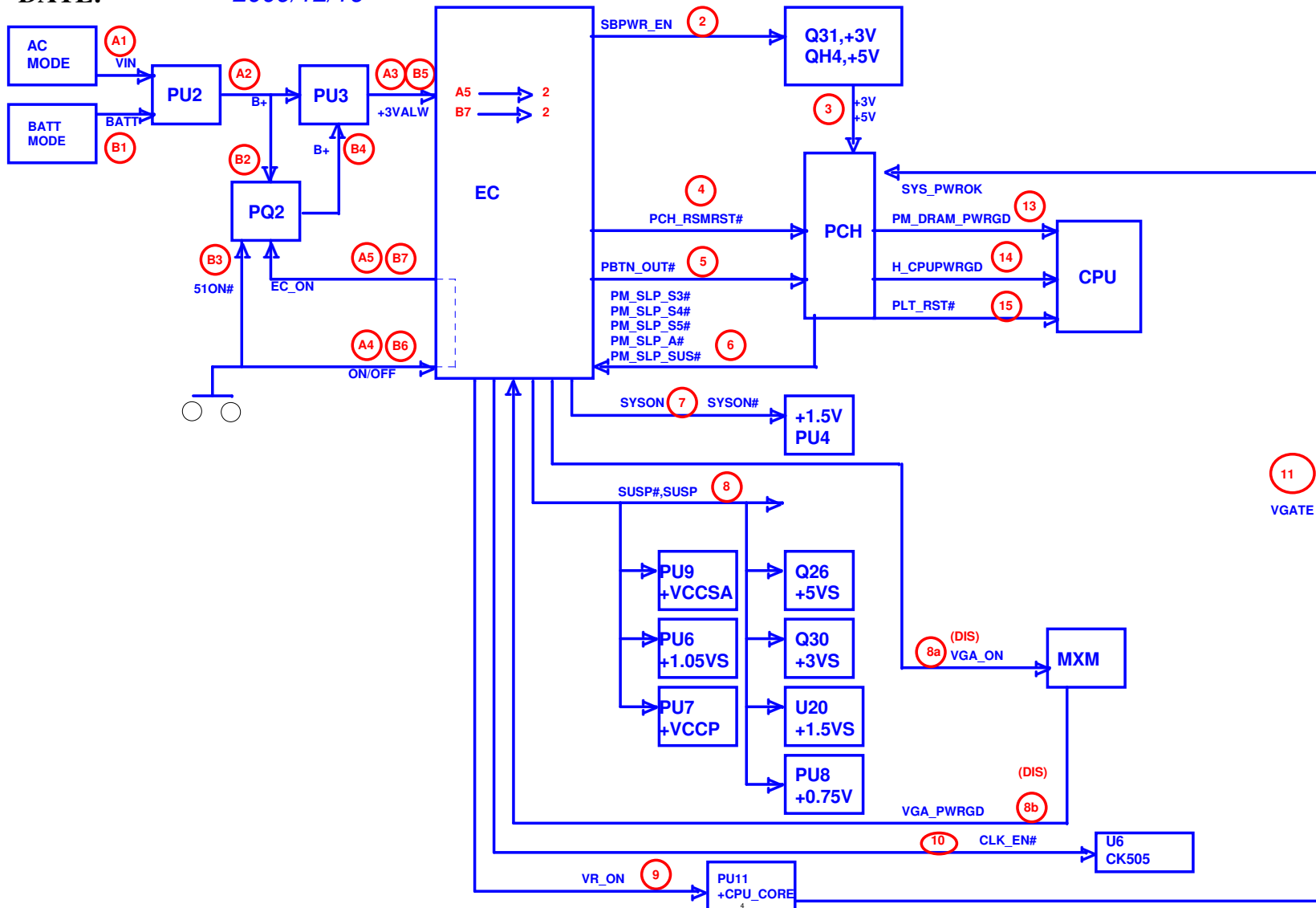
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COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA6691P*
REVISION:
DATE: *2009/12/16*



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1		NECP recommend	0.02	PG#13	EC_LID_OUT#->RH72 change 2.2K to 10K	7/14	PRE-ES1
2		Follow Compal common Design	0.02	PG#28	W_DISABLE#->Remove from EC(3810)	7/14	PRE-ES1
3		Follow Compal common Design	0.02	PG#28	PCH_GPIO28->DEL KC3810(PIN16)	7/14	PRE-ES1
4		Realtek recommend	0.02	PG#25	CA1290-> change 10UF to 2.2UF	7/14	PRE-ES1
5		NEC recommend	0.02	PG#05	Remove RC30~RC34	7/14	PRE-ES1
6		HW Design	0.02	PG#14 PG#21	Change C1554-C1561 to CV77-CV84	7/14	PRE-ES1
7		Follow INTEL CRB	0.02	PG#16	Change RH171 10K to 200K	7/14	PRE-ES1
8		HR_Emeraldlake_CRB_Schem_Fab2 Page4	0.03	PG#05	Change RC13,RC15 from 33ohm to 0ohm	7/21	PRE-ES1
9		HR_Emeraldlake_CRB_Schem_Fab2 Page20	0.03	PG#13	Change RH2111 from 0ohm to 22ohm	7/21	PRE-ES1
10		HR_Emeraldlake_CRB_Schem_Fab2 Page24	0.03	PG#16	Change RH149 from 1Kohm to 2.2Kohm	7/21	PRE-ES1
11		HR_Emeraldlake_CRB_Schem_Fab2 Page24	0.03	PG#16	Change RH150 from 1Kohm to ??ohm	7/21	PRE-ES1
12		HR_Emeraldlake_CRB_Schem_Fab2 Page25	0.03	PG#18	Resever RH189	7/21	PRE-ES1
13		NECP Recommend	0.03	PG#17	ADD CH42 10U	7/21	PRE-ES1
14		NECP Recommend	0.03	PG#14	Delete RH98	7/21	PRE-ES1
15		NECP Recommend	0.03	PG#17	Delete RH261	7/21	PRE-ES1
16		NECP Recommend	0.03	PG#17	ADD LH9 10UH	7/21	PRE-ES1
17		HW Design	0.03	PG#29	Remove Net PCH_VREG_EN#	7/21	PRE-ES1
18		HW Design	0.03	PG#29	Remove Net PCH_PWR_EN	7/21	PRE-ES1
19		HW Design	0.03	PG#29	Remove Net EC_ESB_CLK	7/21	PRE-ES1
20		HW Design	0.03	PG#29	Remove Net EC_ESB_DAT	7/21	PRE-ES1
21		HW Design	0.03	PG#29	Remove Net PCHHOT#	7/21	PRE-ES1
22		HW Design	0.03	PG#29	Remove Net DRAMRST_CNTRL_EC	7/21	PRE-ES1
23		438390_HR_SCH_CHKLIST_Rev1p2	0.04	PG#5	Add RC16 and RC17	7/27	PRE-ES1
24		438390_HR_SCH_CHKLIST_Rev1p2	0.04	PG#10 PG#11	Add QC6 and QC7	7/27	PRE-ES1
25		NECP Recommend	0.04	PG#9	Replace B+_BIAS by +5valw to turn on +1.5V_CPU_VDDQ	7/27	PRE-ES1
26		HW Design	0.04	PG#20	Add sw_config2 to JCRT1.	7/27	PRE-ES1
27	Shift IC	7/27 HW Design					

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		O2 Recommed	0.04	PG#23	Add R1636,R1635,R1630,R1631,R1634 to co-lay OZ888 and OZ600	7/27	PRE-ES1
2		HW Design	0.04	PG#12	Remove clock-gen schematic	7/27	PRE-ES1
3		Follow NECP DRD	0.04	PG#26	Remove Bluetooth schematic	7/27	PRE-ES1
4		Follow NECP DRD	0.04	PG#26	Remove Dimmer schematic	7/27	PRE-ES1
5		Follow NECP DRD	0.04	PG#26	Remove Dipwitch SW1	7/27	PRE-ES1
6		Follow NECP DRD	0.04	PG#27	Remove Gut's card schematic	7/27	PRE-ES1
7		Follow NECP DRD	0.04	PG#27	Change BOM of Gut's card to un-pop.	7/27	PRE-ES1
8		Follow NECP DRD	0.04	PG#28	Remove re-driver of E-Sata.	7/27	PRE-ES1
9		HW Design	0.04	PG#28	Remove EC3810	7/27	PRE-ES1
10		HW Design	0.04	PG#29	Remove sw_config1 from EC3810 to KB930.	7/27	PRE-ES1
11		Follow NECP DRD	0.04	PG#30	Remove C1519-C1544, JKB2.	7/27	PRE-ES1
12		Follow NECP DRD	0.04	PG#30	Remove Express-card schematic.	7/27	PRE-ES1
13		Follow NECP DRD	0.04	PG#31	Remove JESATA	7/27	PRE-ES1
14		Follow NECP DRD	0.04	PG#31	Remove I-POD charge schematic.	7/27	PRE-ES1
15		Follow NECP DRD	0.04	PG#32	Add RU118-RU121, RU1924, RU1928-RU1930, JUSB4, JUSB5 to Co-lay USB2.	7/27	PRE-ES1
16		HW Design	0.04	PG#32	Change to lower-power-version, UPD720200AF1.	7/27	PRE-ES1
17		NECP Recommend	0.04	PG#32	Change SMIB from PIN.H1 to PIN.P4	7/27	PRE-ES1
18		Follow NECP DRD	0.04	PG#33	Remove TEL,EMAIL,INTERNET button.	7/27	PRE-ES1
19		HW Design	0.04	PG#33	Remove power-ok: U124,U125,U127,U128.	7/27	PRE-ES1
20		HW Design	0.04	PG#34	Remove +3VALW to +3V_PCH, add JP5.	7/27	PRE-ES1
21		HW Design	0.04	PG#34	Remove PCH_PWR_EN(Q44).	7/27	PRE-ES1
22		NECP Recommend	0.04	PG#10	Add CD47 and CD48 for SMB	7/27	PRE-ES1
23		NECP Recommend	0.04	PG#11	Add CD49 and CD50 for SMB	7/27	PRE-ES1
24		NECP Recommend	0.04	PG#27	Remove EC_TX and EX_RX from SSD connector to Guts connector.	7/27	PRE-ES1
25		Intel Recommend	0.04	PG#05	Change RC19 1K to 10K	7/27	PRE-ES1

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1		NECP Recommend	0.04	PG#12	Delete RH39	7/27	PRE-ES1
2		NECP Recommend	0.04	PG#16	Delete net SSD_DET PCH GPIO22	7/27	PRE-ES1
3		NECP Recommend	0.04	PG#16	Delete net SSD_DET PCH GPIO57	7/27	PRE-ES1
4		NECP Recommend	0.04	PG#31	Change UU99,UU101 to APL3510	7/27	PRE-ES1
5		NECP Recommend	0.04	PG#32	Change UU105,UU106 to APL3510	7/27	PRE-ES1
6		NECP Recommend	0.04	PG#34	Add R995	7/27	PRE-ES1
7		Intel Recommend	0.04	PG#29	Add U87	7/27	PRE-ES1
8		NECP Recommend	0.04	PG#21	Add RV1532	7/27	PRE-ES1
9		NECP Recommend	0.04	PG#28	Add RS9	7/27	PRE-ES1
10		NECP Recommend	0.05	PG#32	Add Q112 for discharge	7/30	PRE-ES1
11		Intel Check List Rev1.2	0.05	PG#16	Add RH241	7/30	PRE-ES1
12		Intel Check List Rev1.2	0.03	PG#5	Add RC16 and R17	7/30	PRE-ES1
13		HW Design	0.06	PG#12	Add RH32	7/31	PRE-ES1
14		NECP Recommend	0.07	PG#05	Delete RC13,RC15	8/2	PRE-ES1
15		HW Design	0.08	PG#34	Add co-lay of +VCCP to +1.05VS	8/17	ES1
16		NECP Recommend	0.08	PG#21	Add level-shift of HDMI	8/17	ES1
17		Intel Check List Rev1.2	0.09	PG#10,11	Change RD7,RD8,RD11,RD12 to 1k ohms.	8/19	ES1
18		NECP Recommend	0.09	PG#15	Make GPIO55 no connection	8/19	ES1
19		NECP Recommend	0.09	PG#16	Delete RH173.	8/19	ES1
20		NECP Recommend	0.09	PG#5	Delete RC36-RC39.	8/19	ES1
21		NECP Recommend	0.09	PG#31,32	Change UU99,UU101,UU105,UU106 to AP2301MPG-13	8/19	ES1
22		NECP Recommend	0.09	PG#27	Move debug siganl/PCI reset signal to JMINI1.	8/19	ES1
23		NECP Recommend	0.09	PG#24	Change RL453/RL454 from 3.01K ohms to 4.7k ohms.	8/19	ES1
24		NECP Recommend	0.09	PG#25	Change to GND from GND_AMP of JSPK1-G1,G2.	8/19	ES1
25		NECP Recommend	0.09	PG#26	Add dip switch SW1	8/19	ES1
26		NECP Recommend	0.09	PG#25	Change RA1641 from 10k ohms to 10 ohms.	8/19	ES1
27	High of RH69 from +3V_PCH to +3VS.	8/19 NECP Recommend					
28	pin2,pin3 of DH1	8/19 HW Design ES1					

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1		NECP Recommend	0.09	PG#27	Delete DE15 and add RE1667.	8/19	ES1
2		NECP Recommend	0.09	PG#15	Swap USB20_P9 (N9) & USB20_P8 (N8)	8/19	ES1
3		NECP Recommend	0.09	PG#15	Change OC#2 --> OC#5, OC#1 --> OC#6.	8/19	ES1
4		NECP Recommend	0.09	PG#24	Change CL1501,CL1503 to 22U.	8/19	ES1
5		NECP Check List	0.09	PG#20	Add CA1294, CA1295 to EDID	8/19	ES1
6		NECP Check List	0.09	PG#24	Add dis-change circuit of +1.05VS.	8/19	ES1
7		NECP Recommend	0.10	PG#32	Delete "USB3@" of RU2050,RU1746,RU2051,RU1753, CU1422,CU1426.	8/24	ES1
8		NECP Recommend	0.10	PG#22, 23	Delete co-lay of OZ888.	8/24	ES1
9		NECP Recommend	0.11	PG#7	Un-mount RC96/RC97	9/1	ES1
10		NECP Recommend	0.11	PG#27	Add LPC debug signals to JMINI3.	9/1	ES1
11		NECP Recommend	0.11	PG#30	Add power-switch U2 to make the power plane for Human sensor	9/2	ES1
12		NECP Recommend	0.11	PG#30	Add QH9 to prevent leakage.	9/2	ES1
13		NECP Recommend	0.11	PG#29, 30	ADD HS_INT to wake up system.	9/2	ES1
14		NECP Recommend	0.11	PG#15, 27	Add W_DISABLE# to GPIO55 of PCH to inform BIOS the state of RF On/Off.	9/2	ES1
15		NECP Recommend	0.11	PG#21	Remove level-shift of HDMI.	9/2	ES1
16		O2 Recommend	0.12	PG#22, 23	Remove C1255~C1259 Add C1241 and C1235 for PE_3.3VCCA Move C1243 from PE_VCCA to VCCA_OUT and Add C1246 for VCCA_OUT	9/9	ES1
17		HW Design	0.12	PG#21	Remove QV19~QV25.	9/9	ES1
18		437432_HuronRiverPlatform_PSS_1.0_437432	0.12	PG#14, 29	Add R493 and mount RH113 to let RSMRST# disassert and DPWROK assert in the same time.	9/14	ES1
19		NECP Recommend	0.13	PG#5	Add SYSTEM_PWROK to UCL.	9/16	ES1
20		HW Design	0.13	PG#10, 11	Delete RD1,RD4.	9/16	ES1
21		HW Design	0.13	PG#17	Delete RH197.	9/16	ES1
22		HW Design	0.13	PG#32	Change pull high of RU1765 from +3VALW to +3V.	9/16	ES1
23		HW Design	0.13	PG#20	Co-lay QV4.	9/16	ES1
24		HW Design	0.13	PG#21	Reserve DV70~DV72.	9/16	ES1
25		NECP Recommend	0.13	PG#28	Co-lay JP6.	9/16	ES1
26		NECP Recommend	0.13	PG#27	Add DE15 to prevent leakage issue.	9/16	ES1

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1		NECP Recommend	0.13	PG#29	Change pin26 from PCH_DPWROK to WLANPW_DIS#.	9/16	ES1
2		NECP Recommend	0.13	PG#29, 15	Change pin106 from WLANPW_DIS# to W_DISABLE#. Delete W_DISABLE# from GPIO55 of PCH.	9/16	ES1
3		NECP Recommend	0.13	PG#29	Co-lay Pin82 VGATE and PCH_APWROK.	9/16	ES1
4		NECP Recommend	0.13	PG#29	Change pin25 from PCH_APWROK to EC_INV_PWM.	9/16	ES1
5		NECP Recommend	0.13	PG#33	Delete the [SOFT_CTRL], [ZOOM_OUT], [ZOOM_IN].	9/16	ES1
6		NECP Recommend	0.13	PG#20	Mount UV134 to leakage issue.	9/16	ES1
7		NECP Recommend	0.14	PG#7	Delete test points T1-T58.	9/21	ES1
8		HW Design	0.14	PG#28	Remove Co-lay R1541, R1542, R1544, R1545	9/21	ES1
9		NECP Recommend	0.14	PG#30	Add output capacitor C1247 to +5V.	9/21	ES1
10		436735_Huron_River_DG_Rev_1.5	0.14	PG#9	Follow Intel to change RC118, RC119 to 1k ohms.	9/21	ES1
11		436735_Huron_River_DG_Rev_1.5	0.14	PG#12	Follow Intel to add RH25.	9/21	ES1
12		HW Design	0.15	PG#12	Change +3VLP to CHGRTC.	9/24	ES1
13		HW Design	0.16	PG#27	Change pin68 to PWR_BTN_LED#; pin31 to EC_CABC_EN.	9/27	ES1
14		NECP Recommend	0.16	PG#33	JFUN1-25pin delete +3VS.	9/27	ES1
15		NECP Recommend	0.16	PG#29	Add dumping 0ohm of SLP_S4# for AMT debug	9/27	ES1
16		NECP Recommend	0.16	PG#14, 29, 30	Make power plane +3V_HS and +5V_HS which only for Human sensor. Replace SLP_SUS#(pin18 of KB930) by HS_ON to turn on power of Human sensor.	9/27	ES1
17		Intel review result	0.17	PG#24	Change RL44 from 200 ohm to 0 ohm.	9/29	ES1
18		NECP Recommend	0.17	PG#33	Modify pin assignment of LED to along with DRD.	9/29	ES1
19		NECP Recommend	0.17	PG#21	Add RE1670 (1.5M-ohm resistor) around QV108.	9/29	ES1
20		Add HS PW dischargr from NECP Recommend	0.18	PG#30	Change power switch U2/U3 from RT9701 to AP2301	9/30	ES1
21		NECP Recommend	0.18	PG#34	Change JP13 from "0" to "VX0"	9/30	ES1
22		NECP Recommend	0.18	PG#14	Add RH118 to SLP_A# for VX-model don't use this pin.	9/30	ES1
23		NECP Recommend	0.18	PG#14	Add RH2113 to connect PCH_APWROK_R and PCH_PWROK_R.	9/30	ES1
24		NECP Recommend	0.18	PG#14	Move RS1669 and CS1554 to close JMIN11.	9/30	ES1
25		HW Design	0.19	PG#33	Add R2092 for ECO_BTN_CTRL	10/4	ES1
26	for remove A20GATE function.10/5	Intel review result					ES1
27		HW Design	0.20	PG#32	Swap pin1 and pin4 of LU3; swap pin2 and pin3 of LU3.	10/5	ES1

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		ME modify	0.21	PG#32	Change JUSB1&JUSB2 to SANTA_371411-2.	10/6	ES1
2		Intel Recommend	0.22	PG#8	Monut CC130,CC131,CC132,CC134; un-mount CC129,CC133	10/7	ES1
3		NECP Recommend	0.22	PG#9	Change max-voltage of CC176 from 2V to 2.5V.	10/7	ES1
4		ME modify	0.23	PG#32	Change JUSB1&JUSB2 back to SANTA_371394-1.	10/8	ES1
5		HW Design	0.24	PG#26, 34	Change Q40,Q89 from AP2301 to AO3413.	10/13	ES2
6		431433_431433_HR_Emeraldlake_CRB_Schem_Fab2	0.25	PG#13	Change RH68 from 1k to 10k ohms.	10/14	ES2
7		NECP Recommend "reduce S3 power consumption"	0.26	PG#12	Un-mount RH43,RH44,RH45.	10/15	ES2
8		Intel Comment"In DSW disabled system, GPIO27 external pull-down is not required. "	0.26	PG#16	RH241 change to "@"	10/15	ES2
9		HW Design	0.27	PG#29	Change footprint from PL3-A-V-TR-611 to NM302-PL03-GT.	11/03	ES2
10		NECP Recommend	0.27	PG#21	Add CV13,CV15	11/03	ES2
11		NECP Recommend	0.27	PG#15	Change UH3 to TC7SH08FUF_SSOP5.	11/03	ES2
12		NECP Recommend	0.27	PG#12	Add RH1207.	11/03	ES2
13		NECP Recommend	0.27	PG#20	change FV3 to 3A_32V	11/03	ES2
14		NECP Recommend	0.27		change F2,F4,FU5 ,FVI,FV6 to 0.5A_15V_SMD1812P050TF	11/03	ES2
15		HW Design	0.27	PG#20	CV1547 for APL3512A, RV55 for G5243AT11U	11/03	ES2
16		HW Design	0.28	PG#17, 18	Change LH6,LH7,LH9 to SWF20I2CF-I00M for unified material.	11/05	ES2
17		HW Design	0.28	PG#30, 31, 32	Update symbol of U2,U3,UU99,UU101,UU105,UU106	11/05	ES2
18		HW Design	0.28	PG#32	Delete internal clk 48Mhz and RU1900,RU1901,RH2111.	11/05	ES2
19		HW Design	0.28	PG#32	Delete co-lay RU1783,RU1750,RU1758,RU1759.	11/05	ES2
20		ME Design	0.29	PG#30	Add JKB2 and capacitors C1519~C1544.	11/11	ES2
21		HW Design	0.29	PG#32	Change GPIO81&82 to KS016&17. Co-lay W_DISABLE# and TX in GPIO30. Co-lay HS_INT_R and RX in GPIO31.	11/11	ES2
22		NECP Recommend	0.29	PG#12	Un-mount RH271 to disable CABC function.	11/11	ES2
23		HW Design	0.30	PG#27	Change UE93 to AP230IMPG-I3 which has dis-charge function.	11/15	ES2
24		NECP Recommend	0.30	PG#27	Connect pin4 of U3 to GND.	11/15	ES2
25		NECP Recommend	0.30	PG#27	Un-mount RE97.	11/15	ES2
26		NECP Recommend	0.31	PG#27	Mount CE1307,CE1308.	11/18	ES2
27		Vendor Recommend	0.31	PG#24	Change CL529 and CL530 to 18P.	11/18	ES2
28		NECP Recommend	0.31	PG#20 24, 26	Add AND-gate U4,UL18 to PLT_RST#.	11/18	ES2

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		HW Design	0.32	PG#28	Change CS1553,CS1555 to 150U_D_10VM_R40M	11/19	ES2
2		NECP Recommend	0.32	PG#20, 24, 26	mount UL5,U4,RV1201 ;un-mount R168,RL450,RV1200.	11/19	ES2
3		NECP Recommend	0.32	PG#27	Remove LPC BUS(Debug_CLK) from JMINI1.	11/19	ES2
4		NECP Recommend	0.32	PG#29	Mount R488(W_Disable#); unmount R496(EC TX P80 DATA).	11/19	ES2
5		NECP Recommend	0.32	PG#30	Change U2,UE93 from AP2301 to AP2311 for +5V_HS,WLAN	11/22	ES2
6		HW Design	0.5	PG#29	Change R466 15K for Board ID	12/13	PP
7			0.5	PG#30	Add 10KB@/KB@ for VX with 10Key BOM	12/13	PP
8			0.5	PG#20	Change RV120-RV124 to 56ohm for LPC waveform	12/13	PP
9			0.5	21,28	Change RS8, QS1,RE1670,QV108 for NiHM battery	12/13	PP
10			0.5	PG#21	ADD HDMI LS-ASM1442 for EMI	12/13	PP
11			0.5	PG#28	ADD Discharge circuit for +5VS_ODD	12/20	PP
12			0.5	PG#17	Reserve CH41 for verify CRT ripple issue	12/22	PP
13		NECP Recommend	0.5	PG#21	Change RS7 & RV2029 to 300Kohm	12/22	PP
14		HW Design	0.5	PG#16	Add RH173 to distinguish W/10-key from W0/10-key.	12/23	PP
15		HW Design	0.5	PG#28	Change Q40 Vg pull-up power rail to +RTCVREF;Reserve C821	12/27	PP
16		HW Design	0.6		Remove 0ohm resistor and XDP CONN for MRT	02/14	MRT
17		Production line recommend	0.6	PG#34	Modify Jump to 0ohm resistor for factory demand.	02/14	MRT
18		HW Design	0.6	27,34	Modify MiniPCIE and DC/DC BOM structure for MRT	02/14	MRT
19		NECP Recommend	0.6	PG#29	Add UC3 for trigger SYSTEM_PWROK by VGATE	02/22	MRT
20		NECP Recommend	0.6	PG#27	Add QE8 & RE1671 for WLAN LED	02/23	MRT
21		HW Design	0.6	PG#29	Change R466 20K for Board ID	03/04	MRT
22		HW Design	0.6	PG#9	Change Cap. of +VCC_GFXCORE_AXG: Unmount CC157, CC159 & Mount CC158, CC160	03/04	MRT

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